

Total number of printed pages-4

53 (CS 301) COAR

2019

**COMPUTER ORGANIZATION &  
ARCHITECTURE**

Paper : CS 301

Full Marks : 100

Time : Three hours

**The figures in the margin indicate  
full marks for the questions.**

Answer **any five** questions.

1.

(a) Convert the following :

(i)  $(193)_{10} = (X)_2$

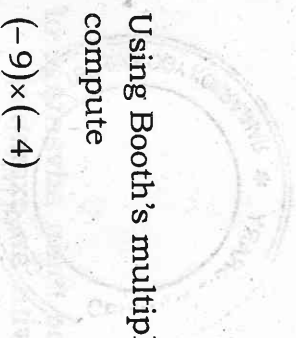
(ii)  $(1101011)_2 = (X)_8$

(iii)  $(1101.101)_2 = (X)_{10}$

(iv)  $(CD9)_{16} = (X)_2$

(v)  $(473)_8 = (X)_{16}$

Contd.



(b) With an example discuss about the IEEE floating point representation technique. (Clearly mention the storing and reading operations).  $2 \times 5 + 10$

3. (a) Using Booth's multiplication algorithm, compute  $(-9) \times (-4)$

2. Design a CPU capable of performing the following operations :

(b) Using non-restoring division algorithm compute  $15/4$

- (i) ADD
- (ii) Subtract
- (iii) Multiply
- (iv) Division
- (v) Greater than
- (vi) Less than
- (vii) AND
- (viii) OR

4. (a) With a diagram discuss a static RAM cell. How ROM cell differs from a RAM cell ?

and has 8 registers  $R_0, R_1, \dots, R_7$ . Clearly show your control signals.  
Compute the control signals for the following instructions :

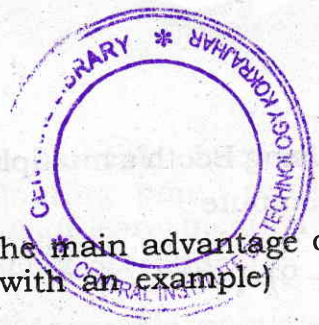
ADD  $R_0, R_1, R_2 // C(R_0) \leftarrow C(R_1) + C(R_2)$

LT  $R_1, R_2, R_3 // \text{if } C(R_2) < C(R_3)$

$C(R_1) \leftarrow C(R_2)$   
else  
 $C(R_1) \leftarrow C(R_3)$       20

(b) Consider a RAM having of 8192 blocks and each block contains 16 words. The cache memory size is 256 blocks (32 words).  
Compute the parts of the CPU address for the following cache mapping techniques :

- (i) Direct
- (ii) Associative
- (iii) 2 Ways Set Associative.       $5 + 3 \times 5$



5. 20
- (a) What is the main advantage of DMA? (Discuss with an example)
  - (b) Write the differences between programmed I/O vs Interrupt driven I/O. According to your opinion, which one is suitable for our modern computer?
  - (c) With an example discuss about priority interrupt.
6. (a) What are the advantages of pipelining?
- (b) Consider a computer uses five stage pipelining. Each stage needs 5ms. If you have 1000 instructions then compute the speed up.
- (c) What are the different hazards in pipelining? 5+5+10
7. Write short notes on: 5×4
- (a) PC
  - (b) Virtual Memory
  - (c) Immediate addressing mode
  - (d) Stored program architecture.