53 (CS 301) COAR

2017

COMPUTER ORGANIZATION AND ARCHITECTURE

Paper : CS 301

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* What is von-Neumann stored program concept ? Describe using suitable diagram. How performance of a processor can be improved ?

8+2=10

(b) Write use of the following registers : PC, IR, MAR and MDR. Write typical operating steps to execute a program in a computer. 4+6=10

7. Write short notes on : 5×4=20

(a) RISC

(b) RAID

(c) DMA

(d) Hardwired Control.

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2. *(a)* Define the term 'microoperation' in the context of digital system. What is register transfer language ? Write following micro operations using register transfer language syntax : register transfer, simultaneous transfer, conditional transfer. 2+2+6=10

(b) What is a bus ? Design a bus system to transfer data from four registers using common bus. Assume 4-bit computer. 2+8=10

3. *(a)* Write briefly about *five* different types of addressing modes. If the size of the address bus is 16 bit and each memory location can store 1 byte of data then what can be the size of the main memory ? 5+5=10

(b) What is Virtual Memory ? Explain the concept of page and frame. 2+8=10

4. *(a)* Determine the decimal value of 10001011 in signed magnitude representation and in two's complements representation. 5+5=10

(b) How real numbers are represented in computer ? Describe. Convert 6·75 into IEEE single precision floating point representation. 5+5=10

5. (a) Draw basic organization of a microprogrammed control and define the terminologies related to microprogrammed control unit. 10

(b) Explain program controlled I/O and interrupt driven I/O. 5+5=10

6. (a) What is Pipelining ? Explain about 4-stages pipelining. 10

(b) Draw the block diagram of a tightly coupled multiprocessor system and explain in brief. What is Cache Coherence Problem ? Describe. 5+5=10