Total No. of printed pages = 5

Co-605/VLSI&ES/6th Sem/2018/M

# VLSI AND EMBEDDED SYSTEMS

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

## PART – A

Marks – 25

1. Which of the following integration technology is the fastest ? 2

   (a) NMOS (b) PMOS

   (c) CMOS (d) Bipolar

2. The designer of an IC transforms a circuit description into a geometric description, called as 2

   (a) Layout (b) Wafer

   (c) Chip (d) System

[Turn over

3. The process of a creating a specified pattern on the wafer through a mask is called 2

(a) Physical design (b) Chip design

(c) Photo-lithography (d) Masking

4. In standard cell based design, cells are placed in rows and the space between two rows is 2

(a) Route (b) Channel

(c) Channel length (d) Feedthrough

5. Geometrical dimensions and spacing of each blocks is specified in which step of design cycle ? 2

(a) Logic design (b) Fabrication

(c) Functional design (d) Physical design

6. Fill in the blanks with suitable words : 1×5=5

(a) FPGA stands for ———.

(b) Connection between horizontal segments is provided through ——— in an FPGA.

(c) An NMOS transistor is said to be ON, when ———.

(d) Physical design step of VLSI design cycle has ——— substeps.

(e) Full form of DRC is ——— .

7. Indicate whether the following are true or false : 1×5=5

(a) The objective of the routing phase is to complete the interconnections between blocks according to the specified netlist.

(b) The input to the physical design cycle is a circuit diagram and the output is the layout of the circuit.

(c) The design cost of a Full-custom design style is lowest as compared to other design styles.

(d) In the Von-Neumann architecture, the L1 cache is often divided into an instruction cache and a data cache, but the Harvard architecture has a single cache.

(e) CMOS technology provides higher integration density compared to Bipolar and Bi-CMOS technology.

8. (a) Which design style allows functional blocks to be of any size ?

(b) Which block receives signals both from the sensors of the physical device and user interface in general embedded system ?

(c) Which one out of NMOS and PMOS transistor passes the logic '1' efficiently ?

(d) What do mean by scaling in VLSI ?

(e) Define static power dissipation. $1 \times 5 = 5$

PART – B

Marks – 45

9. Draw the design flow of VLSI systems. Describe the physical design and fabrication step. $4+3+3=10$

10. Describe the Semi-custom based VLSI design with proper diagrams and write how is it different from Full-custom based design. $8+2=10$

11. (a) Write down the process sequences for NMOS technology.

(b) Define the static power dissipation, dynamic power dissipation and short circuit power dissipation in CMOS technology. 6+3=9

12. Compare the performance and features of RISC and CISC processors. 5+5=10

13. Discuss the Von-Neumann architecture of processors for embedded systems. 6