Total No. of printed pages = 3

Co-605/VLSI&ES/6th Sem/2013/M

VLSI AND EMBEDDED SYSTEM

Full Marks – 70

Pass Marks – 28

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer question No.1 and any *five* from the rest.

1. (a) What is a stimulus ? 1

   (b) Define partitioning in VLSI design. 1

   (c) Define optimal scheduler and give one example of optimal real time scheduling algorithm. 1+1=2

   (d) Why ASICs are used in Embedded system ? 2

   (e) State Moore's law. 2

   (f) Give one example each of Hard Real Time system and Soft Real Time system. 2

[Turn over

(g) Why PCs are not considered to be an Embedded system ? 2

(h) Differentiate between deadline and delay. 2

(i) When RMA is not optimal static priority scheduling algorithm ? 1

2. Describe architecture of an Embedded system with a diagram. 11

3. Why floor planning is necessary in VLSI ? Describe Time Driven Floor Planning technique. 3+8=11

4. What is clock drive scheduling ? Describe DMA real time scheduling algorithm with one example. 4+7=11

5. Why FPGAs are used in VLSI ? Explain the FPGA blocks. 3+8=11

6. (a) What are the various VLSI technologies ? Mention advantages and disadvantages of CMOS technology. 2+4=6

(b) Why design rule checking is necessary in VLSI design ? Explain DRC technique. 2+3=5

7. What are the types of RTS ? Give one example of RR deadline constraint model the example with FSA. 4+2+5=11

8. Write short notes on any *two* of the following topics : 11

(i) Hardware software codesign

(ii) Real Time Communication

(iii) Embedded system validation techniques

(iv) Levels of Partitioning.