Total No. of printed pages = 6

END SEMESTER EXAMINATION – 2019

Semester : 6th

Subject Code : Co-604

PARALLEL PROCESSING

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Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Instructions :

1. Questions on PART–A are compulsory.
2. Answer any *five* questions from PART–B.

PART – A

Marks – 25

Choose the correct answer : 1×10=10

1. IC (Integrated Circuit) was first introduced in
   (a) First generation of computer
   (b) Second generation of computer
   (c) Third generation of computer
   (d) Fourth generation of computer

[Turn over

2. Speed up in a computer is required because of

(a) Low price of computers

(b) Complex computation

(c) Solving simple mathematical problems

(d) None of the above

3. An array computer has an

(a) Array of Hard Disks

(b) Array of RAMs

(c) Array of PEs

(d) Array of I/O devices

4. DMA is the abbreviation of

(a) Digital Memory Analysis

(b) Digital Memory Access

(c) Direct Memory Access

(d) Direct Memory Analysis

5. Cache memory works based on the principle of

(a) Locality of reference

(b) Locality of interference

(c) Propositional logic

(d) Scanning based approach

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6. Paging is used to convert

(a) Page address to segment address

(b) Segment address to page address

(c) Physical address to logical address

(d) Logical address to physical address

7. Write through protocol is related with

(a) Cache mapping (b) Page replacement

(c) Disk scheduling (d) Cache coherence

8. Which pipelining technique can effectively be used to design a floating point multiplier without increasing the number of processors ?

(a) Arithmetic (b) Functional

(c) Processor (d) None of the above

9. Consider the two following instructions

$X = 20$

$Y = X+3$

If both these instructions are executed in a four stage pipeline processor what type of hazard will occur ?

(a) Data hazard

(b) Functional hazard

(c) Instruction hazard

(d) None of the above

10. Out the following four types of computer which one is most powerful ?

(a) SISD (b) SIMD

(c) MISD (d) MIMD

11. Fill in the blanks : 1×5=5

(a) IBM stands for _____.

(b) TLB stands for _____.

(c) Cache memory is a _____ type of memory.

(d) AI is developed in _____ generation.

(e) Hit ratio of cache memory = _____

12. Write true or false : 1×5=5

(a) Pipelining can be used in floating point multiplier design.

(b) LRU is a cache mapping technique.

(c) Page table contains the mapping of logical address to physical address.

(d) Parallelism can exist in a SISD processor.

(e) There is a requirement of clock for the design of any pipeline processor.

13. Match the followings : 1×5=5

Column – A	Column – B
(a) Batch Processing	(i) Flynn's classification
(b) SISD, SIMD, MISD, MIMD	(ii) Hardwire
(c) Cache Memory	(iii) Operating System
(d) Read after Write	(iv) Speed up in parallel computers
(e) Minsky's conjecture	(v) Hazards

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PART– II

Marks – 45

14. With suitable diagrams discuss about

(a) SISD

(b) SIMD and

(c) MIMD Processors. 3+3+3=9

15. (a) Compare between parallelism and pipelining.

(b) "Number of stages in pipelining is a determining factor for speedup". — Justify the statement. 5+4=9

16. (a) What is the necessity of cache memory in a computer ?

(b) Consider a direct cache mapping technique. The word size in cache and main memory is 32. If the cache contains 128 blocks and main memory contains 4096 blocks then compute the different parts of the address generated by the processor. 5+4=9

17. With suitable diagram discuss the following networks : 3+3+3=9

(a) Shuffle exchange

(b) Butterfly

(c) Cube

18. With examples discuss the different hazards of pipelining. 9

19. With an example discuss about the memory interleaving technique. 9

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