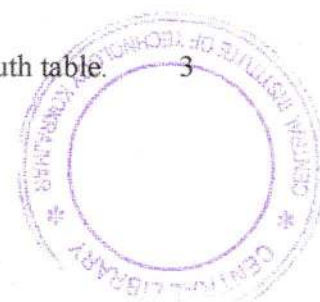


END SEMESTER/ RETEST EXAMINATION, 2020**Semester: Fourth****Subject code: Co-406(NEW)****Subject: Digital Electronics****Full Marks: 35****Duration: Three hours****PART-A****MARK-25**

1. Fill in the blanks: 1x5=5
- Signed bit is _____ of a signed binary number.
 - TTL is _____.
 - In _____ code only one bit change is occur at a time.
 - In 4X1 MUX has _____ inputs and _____ output.
 - D Flip Flop is known as _____.
2. Write true or false: 1X5=5
- The output of NAND gate is high when both the inputs are high.
 - SOP is sum of product.
 - Sequential circuit does not have memory element.
 - In S-R Flip Flop $S=R=1$ is permitted.
 - ADC is analog to digital converter.
3. Choose the correct answer 1X4=4
- NAND is the combination of-
 - NOT and AND
 - NOR and AND
 - NOT and NAND
 - NOR and EX-OR
 - FET is-
 - Field energized transistor
 - field effect transistor
 - fast effect transistor
 - fast energized transistor
 - DE-MUX has-
 - Several input and one output
 - one input several output
 - four input four output
 - one input four output
 - Output of EX-NOR gate is-
 - $AB+A'B$
 - $A'B+AB'$
 - $2AB$
 - $A+B$

PART-B**Answer any three questions from 4-7**

4. a) Draw the logic symbols of NOR gate and Ex-OR gate, write its truth table. 3



- b) perform the following— 4
- i) find the decimal equivalent of binary number $(11111001)_2$
 - ii) express AF.9B hexadecimal number into its binary equivalent
 - iii) perform following operation using 2's complement method 48-23
5. a) what is half subtractor ? Draw its logic symbol and write truth table. 3
- b) Implement the expression using MUX $f(A,B,C,D) = \sum m(0,2,5,7,11,14,16)$. 4
6. a) Draw the logic symbol of JK Flip flop write its truth table. 3
- b) Draw and write briefly the logic diagram of master slave flip-flop . 4
7. a) Draw the response of transient and steady state along with steady state error. 3
- b) Draw and reduce the karnaugh map for the following function 4
 $F(A,B,C,D) = \sum m(0,1,3,4,6,9,11,13)$
8. a) Write briefly about about display device. 3
9. a) draw the logic symbol of asynchronous UP-DOWN counter. 3
10. Draw the diagram of shift register. 3

