END SEMESTER/ RETEST EXAMINATION, 2020

Semester: Fourth

Subject code: Co-406(NEW)

Subject: Digital Electronics

Full Marks: 35

Duration: Three hours

PART-A

MARK-25

1. Fill in the blanks: 1x5=5
   a) Signed bit is_____ of a signed binary number.
   b) TTL is___.
   c) In __ code only one bit change is occure at a time.
   d) In 4X1 MUX has___ inputsand ____ output.
   e) D Flip Flop is known as_____.

2. Write true or false: 1X5=5
   a) The output of NAND gate is high when both the inputs are high.
   b) SOP is sum of product.
   c) Sequential circuit does not have memory element.
   d) In S-R Flip Flop S=R=1 ispermitted.
   d) ADC is analog to digital converter.

3. Choose the correct answer 1X4=4

a) NAND is the combination of-
   i) NOT and AND ii) NOR and AND iii) NOT and NANDiv) NOR and EX-OR

b) FET is-
   i) Field energized transistor ii) field effect transistor iii) fast effect transistor iv) fast energized transistor

c) DE-MUX has-
   i) Several input and one outputii)one input several output iii)four input four output iv)one input four output

d) Output of EX-NOR gate is-
   i) AB+A`B`ii)A`B+AB`iii)2ABiv)A+B

PART-B

Answer any three questions from 4-7

4. a) Draw the logic symbols of NOR gate and Ex-OR gate ,write its truth table. 3

b) perform the following– 4

i) find the decimal equivalent of binary number $(11111001)_2$

ii)express AF.9B hexadecimal number into its binary equivalent

iii) perform following operation using 2's compliment method 48-23

5. a) what is half subtractor ? Draw its logic symbol and write truth table. 3

b) Implement the expression using MUX $f(A,B,C,D) = \sum m(0,2,5,7,11,14,16)$. 4

6. a)Draw the logic symbol of JK Flip flopwrite its truth table. 3

b) Draw and write briefly the logic diagram of master slave flip-flop . 4

7. a) Draw the response of transient and steady state along with steady state error. 3

b) Draw and reduce the karnaugh map for the following function $F(A,B,C,D)=\sum m(0,1,3,4,6,9,11,13)$ 4

8. a) Write briefly about about display device. 3

9. a) draw the logic symbol of asynchronous UP-DOWN counter. 3

10. Draw the diagram of shift register. 3

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