END SEMESTER/RETEST EXAMINATION, 2020 (New)

Semester: 3rd

Subject code:CO -303

Subject:Computer Architecture and Organization

Full Marks: 70(part A-25 + Part B-45)

Duration: 3 hours

Instructions:

1. *Questions on Part A are compulsory*
2. *Answer any 5(five) questions from Part B*

Part A

Question no.	Questions	Marks
Question 1	**Choose the correct answer**	1x10=10
a)	In D flip-flop, D stands for a) Distant b) Delay c) Desired d) None of the Mentioned	
b)	The instructions like MOV or ADD are called as a)OP-Code b)Operators c)Commands d) None of the mentioned	
c)	How many AND gates are required to realize Y = CD + EF + G ? a) 4 b) 5 c) 3 d) 2	
d)	The addressing mode, where you directly specify the operand value is a)Immediate b) Direct c) Definite d) Relative	
e)	PROM stands for a) Programmable Read Only Memory b) Pre-fed Read Only Memory c) Pre-required Read Only Memory d) Processor Read Only Memory	
f)	To reduce the memory access time we generally make use of a) Heaps b) RAM c) SDRAM d) Cache	
g)	The DMA transfers are performed by a control circuit called as	

	a) Device interface b) DMA controller c) Data controller d) Over looker	
h)	The memory device that is generally made of semi-conductor is a) RAM b) Hard-disk c) Floppy disk d) C D	
i)	The ALU makes use of _____ to store the intermediate results. a)Heap b) Registers c) Accumulators d) Stack	
j)	_____ is generally used to increase the apparent size of physical memory. a) Secondary memory b) Virtual memory c) Hard-disk d) Disks	
Q2	**State true or false:**	1x10=10
a)	The NAND gate is AND gate followed by NOT gate.	
b)	The decimal numbers represented in the computer are called as floating point numbers, as the decimal point floats through the number.	
c)	An universal logic gate is NAND gate.	
d)	In the memory hierarchy, as the speed of operation increases the memory size also increases.	
e)	Status registers are also calledFlags.	
f)	ROM is an erasable memory.	
g)	Actual execution of instruction in a computer takes place in Control Unit.	
h)	In memory-mapped I/O, the I/O devices and the memory share the same address space.	
i)	Hard disk is a main memory device.	
j)	Micro programmed control unit is input device.	
Q3	**Fill in the blanks**:	1x5=5
a)	Floating point representation is used to store _____numbers.	
b)	The NOR gate output will be high if the two inputs are _____	
c)	DMA stand for _____	
d)	In memory hierarchy _____are at the top level	
e)	Scanner is a _____ device	

Part B

Answer any five (5) questions from Part B

Question no.	Questions	marks
4 a)	Write briefly about Von Neumann Architecture.	3
b)	Represent the circuit diagram and truth table of D flipflop	3
c)	Draw the Logic circuit of the following. i) A +AB + ABC ii) (XY+Z) (Y+Z)(ZY+X)	3
5 a)	What are computer registers? Name them and write their purposes.	4
b)	What do you mean by addressing mode ? Define direct Addressing mode and immediate addressing mode.	2+3=5
6 a)	What do you mean by instruction format?	2
b)	Write briefly about stack organization.	3
c)	Write briefly about Hardwired control unit.	4
7a)	Differentiate ROM and RAM.	3
b)	What do you mean by Memory Hierarchy? Explain briefly about cache memory.	3+3=6
8a)	What is DMA ?	2
b)	Explain briefly the working principle of Virtual memory.	4
c)	Differentiate between memory mapped I/O and Isolated I/O.	3
9 a)	Explain Booth's algorithm to multiply two numbers in 2's complement form.	4
b)	Use the Booth's algorithm to multiply -12 decimal with -10 decimal.	5
10 a)	Write brief notes on Programmed I/O and interrupt initiated I/O	5
b)	Write a brief note on Printer.	4
11	**Write short notes on (Any 3)** a)Multiplexer b)Encoder c) Half Adder d)Flags e)Priority Interrupt	3 X 3 =9

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