CAI-505/M&A/5th Sem/2018/M

MICROPROCESSORS AND APPLICATIONS

Full Marks - 70

Time - Three hours

The figures in the margin indicate full marks for the questions.

The Question Paper consists of two parts: PART-A and PART-B. Both are compulsory.

PART-A

(Marks - 25)

All questions are compulsory.

- 1. Answer the following questions within one sentence: $1 \times 10=10$
 - (i) What is a machine language?
 - (ii) Define the term "Word".
 - (iii) What is the function of Stack pointer in 8085 microprocessor?
 - (iv) How many address lines are required to address 2KB memory?

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| (v) What is the need of the \overline{WR} signal on memory chip? | | | | | |
|---|--|--|--|--|--|
| (vi) Why 8085 is called 8-bit processor? | | | | | |
| (vii)Specify the numbers of registers and memory cells in a 128 × 4 memory chip. | | | | | |
| (viii) State the function of IO/\overline{M} signal of 8085 microprocessor. | | | | | |
| (ix) Why the bus AD_7 - AD_0 has to be demultiplexed? | | | | | |
| (x) What is the maximum number of input-output devices that can be connected in 8085 using Memory mapped I/O technique? | | | | | |
| Fill in the blanks: 1×5=5 | | | | | |
| (i) The OUT is a byte instruction. | | | | | |
| (ii) A tristate buffer is commonly used to interface devices. | | | | | |
| (iii) A group of 4 bits is called | | | | | |
| (iv) The number of flags in ALU are | | | | | |
| (v) The largest positive integer that can be processed by 8085 at one time is | | | | | |

| 3. | 3. Choose the correct answer: | | |
|----|-------------------------------|------------------------------------|---|
| | (i) | The microprocesso it fetches as an | r interprets the first byte |
| | | (a) Opcode | (b) Operand |
| | | (c) Port address | (d) Register |
| | ii) | Example of data t | ransfer (copy) instruction |
| | | (a) ADD R | (b) STA 16 - bit |
| | | (c) ANA R | (d) CALL 16 - bit |
| | iii) | The size of the in | nstruction "RLC" is |
| | | (a) 1-byte | (b) 2-byte |
| | | (c) 3-byte | (d) 4-byte |
| | iv | | ddress (d) Register of data transfer (copy) instruction R (b) STA 16 - bit R (d) CALL 16 - bit of the instruction "RLC" is (b) 2-byte (d) 4-byte the following is used for temporary f binary information? Disk (b) RAM (d) Stack |
| | | (a) Hard Disk | (b) RAM |
| | | (c) ROM | (d) Stack |
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- (v) The instruction SUB A will clear the
- (a) Program counter
 - (b) Stack pointer
 - (c) Accumulator
 - (d) None of the above.
- 4. Match the following in column A with the correct answer from column B: 1×5=5

| Column A | Column B |
|-------------------|----------------|
| Read/Write Memory | Keyboard |
| Output device | Windows 10 |
| Address bus | 7 segment LEDs |
| Operating system | Unidirectional |
| Input device | RAM |

PART-B

Marks - 45

Answer any five (5) questions.

5. (a) Draw a block diagram of a computer with the microprocessor as CPU.

- (b) Define opcode and operand, and specify the opcode and operand of the following instructions-
 - (i) MOV A, B (ii) STA 3000H
- (c) How does a microprocessor differentiate between an Opcode and data? 2
- 6. Draw a neat and clean functional block diagram of 8085 microprocessor. List the various internal units that make up 8085 architecture, and explain their functions in decoding and executing an instruction.
- 7. (a) What will be the output of the following program? Also assemble the program starting with memory address C000H:

SUB A

MOV B, A

DCR B

INR B

SUI 01H

HLT

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(b) If the 8085 adds 87H and 79H, specify the contents of the accumulator and the status of the S, Z, and CY flags.

8. (a) Write an assembly language program to exchange the content of reg B with content of reg C. Load EAH in register B and CDH in register C. Also draw the flow chart.

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- (b) Identify the machine cycles in the following instructions:

 - (i) ADD B (ii) XRI 8-bit data
 - (iii) STA 16-bit (iv) CMA

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9. (a) In Fig.1 design the chip select logic Hardware with NAND gates so that the memory address range will be as indicated.

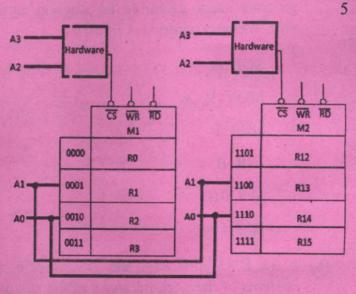
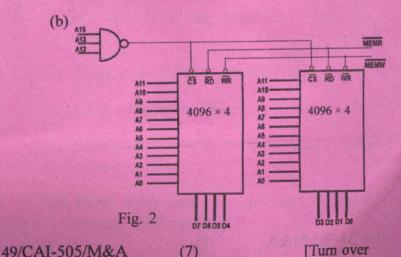


Fig. 1

(b) Assemble the following program starting with memory address C050H and specify the total number of bytes consumed:

MVI A, FFH
MVI B, 01H
SUB B
XRA A
STA 3050H
RST1

- 10. (a) Design a memory interfacing circuit with the following components:
 - > 3 to 8 decoder (with enable inputs $\overline{E_1}$, $\overline{E_2}$ and E_3)
 - > 2Kbyte EPROM
 - > The address range should begin with 3000H.



Identify the don't care address line and specify the entire memory map of the schematic shown in fig. 2.

 (a) Make a comparison between Memory mapped I/O and I/O mapped I/O interfacing schemes.

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- (b) List the different 8085 interrupts and their vector locations.
- 12. (a) Differentiate the following:
 - > High level language and low level language.
 - ➤ Instruction cycle, Machine cycle and T-states.
 - (b) Draw the timing diagram of MVI instruction.

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