Total No. of printed pages = 4

CAI-303/Digital Circuits/3rd Sem/2014/N

DIGITAL CIRCUITS

Full Marks – 70

Pass Marks – 28

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer any *five* questions.

1. (a) Using Boolean algebra, simplify the following expressions as much as possible. 2×2=4

   (i) $A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C$

   (ii) $AB + \overline{AB}\,C + A$

   (b) Draw the logic circuit represented by below expression

   $Y = A + B\,[\,C + D(B + \bar{C})]$ 3

   (c) Use K-map method to simplify the following Boolean function : 5

   $Y = f(w, x, y, z) = \sum m\,(0, 2, 4, 5, 8, 10, 12, 14, 15)$

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(d) (i) Convert $(1001)_2$ to decimal.

(ii) Convert $(DAF1)_{16}$ to binary. 1×2=2

2. (a) Show how the following expressions can be implemented using NAND gate only.

(i) $Y = ABC$ (ii) $Y = \overline{ABC}$. 3×2=6

(b) Show how the following expressions can be implemented using NOR gate only.

(i) $Y = A + B$ (ii) $Y = A + B + \overline{C}$ 3×2=6

(c) Use basic gates to implement $Y = AB + \overline{B}C$. 2

3. (a) Implement Half Adder logic circuit. 5

(b) Show how a 2 to 4 decoder logic circuit can be implemented starting from its truth table. 5

(c) (i) Convert decimal 26 to BCD. 1×2=2

(ii) Convert BCD 10101011 to decimal.

(d) Apply DeMorgan's law to

$$Y = \overline{\overline{A+\overline{B}+\overline{C}} + \overline{d}.\overline{b}}$$ 2

4. (a) Design a 4:1 multiplexer logic circuit starting from its function table. 6

(b) Describe the truth table of a S-R latch. 3

(c) Draw the logic diagram of J-K latch and describe its truth table. 3+2=5

5. (a) Draw the block diagram of 2 bit binary parallel adder. 3

(b) Use 1's complement method to perform the subtraction 1010 – 0100. 3

(c) Use K-map method to simplify
$Y = f(x, y, z) = \sum m(0, 2, 4)$ with don't care conditions d (3, 5). 5

(d) Convert f(x, y, z) = xy + x'y' to cannonical SOP form. 2

(e) 2's complement of 10010001 is 1

6. (a) Explain the operation of a 2 bit ripple counter with block diagram, timing diagram. 7

(b) What are the main differences between synchronous and asynchronous logic ? 3

(c) Describe the truth table of D-latch. 3

(d) Multiplied value of 101×11 is 1

7. (a) Implement full subtractor circuit. 7

(b) Design a 4 to 2 encoder logic circuit starting from its truth table. 5

(c) Convert $(243)_8$ to binary. 1

(d) Convert $(40)_{10}$ to binary. 1