Total No. of printed pages = 6

CAI-303/DC/3rd Sem/2017/N

DIGITAL CIRCUITS

Full Marks – 70

Pass Marks – 28

Time – Three hours

The figures in the margin indicate full marks for the questions.

PART – A

Marks – 25

All the questions are compulsory.

1. (i) Convert the following : 4

(a) $(35)_{10} = (\ldots\ldots)_2$

(b) $(AF0)_{16} = (\ldots\ldots)_2$

(c) $(1001.01)_2 = (\ldots\ldots)_{10}$

(d) $(D10)_{16} = (\ldots\ldots)_{10}$

[Turn over

(ii) Answer the following questions : $1 \times 10 = 10$

(a) Obtain the 2's compliment of 000101.

(b) Represent the decimal number 72 in BCD code.

(c) Number of control inputs needed to implement 16:1 multiplexer is _____.

(d) Write down 2 bit gray code sequence .

(e) 1111 × 101 = _____.

(f) Number of inputs present in 1:8 demultiplexer is _____.

(g) Binary to gray code conversion of 010111 is _____.

(h) Find out the max term if the variables a,b,c,d,e is talking values 0,1,0,0,1.

(i) Subtracted value of 10110 – 01101 is _____.

(j) How many minimum NAND gate is needed to implement x-or operation.

(iii) Write down whether the following statements are true / false : $1 \times 11 = 11$

(a) D - latch is a combinational circuit.

(b) a+b= b + a is an example of commutative law.

(c) Multiplexer is a data selector circuit.

(d) Full Adder can be used to add 2 bits.

(e) 3 bit counter can count upto 16.

(f) Asynchronous circuit uses external click to enable all the circuits.

(g) Master slave flip fop removes race around condition.

(h) abc + (abc)' = 0.

(i) Ex-3 code of 56 is : 101110.

(j) (x'y'z')' = xyz.

(k) (x+x'y') (x+x'y) = x.

PART – B

Answer any *three* questions.

1. (i) Simplify using boolean algebric method. $2 \times 2 = 4$

(a) abc' + ab'c' + a'b'c + ab'c + a'bc

(b) {(x+y'+z')' + (x'y'z)' + xy}'.

(ii) Simplify using K-map method : 5+6=11

(a) $f(w,x,y,z) = \Sigma m(0,2,4,5,6,9,11,12,13)$

(b) $f(a,b,c,d) = abcd + adcd' + a'b'c'd + abc'd + a'b'cd + a'bcd' + ab'c'd.$

2. (i) Use basic gates to implement $Y = ab'(c+d') + a'b(c'+d)$. 3

(ii) Use NAND gate only to implement $Y = ab + cd'$. 4

(iii) Prove that $(a+b+c)' = a' + b' + c'$. 3

(iv) Why NAND, NOR gates are called universal gate. 2

(v) Write down distributive, commutative, associative law of Boolean algebra. 3

3. (i) Design a Full Subtractor. 6

(ii) Write down truth table of a 2 to 4 Encoder. 2

iii) Write down function table of a 8:1 Multiplexer. 2

(iv) Distinguish between combinational and sequential circuit. 3

(v) Use Nor gate only to implement $Y = ab$ 2

4. (i) Explain the operation of S-R latch with circuit diagram, truth table. 4

(ii) Draw the logic diagram of a J-K latch. 2

(iii) Explain the operation of a master slave flip flop with logic diagram, truth table. 5

(iv) Explain 2 bit ripple carry adder with block diagram. 4

5. (i) Describe the function of a 2 bit Counter with block diagram, timing diagram. 8

(ii) Draw the logic diagram of a D latch. 2

(iii) Design a 1 : 8 De-Multiplexer. 5

6. (i) Use 2's Complement method to subtract 1110 – 1001. 2

(ii) Describe the function of a 4 bit Register with block diagram, timing diagram. 8

iii) Write down BCD and Ex-3 code of decimal 34. 2

(iv) What do you mean by binary coding ? Explain with example. 3

7. (i) Simplify using K-map method : 6

$f(w,x,y,z) = \Sigma m(0,2,4,5,6,9,12,13) + d(1,3,10)$

(ii) Define the following : $2 \times 4 + 1 = 9$

(a) Logic gate (b) Half-Subtractor

(c) Multiplexer (d) Decoder

(e) Encoder.