Total No. of printed pages = 4

CAI-303/DC/3rd Sem/2016/N

DIGITAL CIRCUITS

Full Marks – 70

Pass Marks – 28

Time – Three hours

The figures in the margin indicate full marks for the questions.

Answer any *five* questions.

1. (a) Convert the following : 1×5=5

(i) $(2F1)_{16} = (?)_2$

(ii) $(1A1)_{16} = (?)_{10}$

(iii) $(101011)_2 = (?)_8$

(iv) $(123)_8 = (?)_{10}$

(v) $(101111)_2 = (?)_{10}$

(b) Perform addition 1

10101 + 10110

(c) Subtract using 2's complement method 2

1011 – 1000

[Turn over

(d) State De-Morgan's law of Boolean algebra. 2

(e) Simplify using Boolean algebra 4

$f(x,y,z) = (x+y)(x+yz)(x+y'z)(x+y)'(x+x)'$

2. (a) Simplify using K-map method 5

$f(w, x, y, z) = \sum m(0, 1, 2, 3, 8, 9, 10, 11) + d(13, 14)$

(b) Why NAND, NOR gates are called universal gates ? 2

(c) Use basic gates only to implement the below Boolean equation 3

$Y = f(a, b, c) = ab'c + (a + b)(c' + d)$

(d) Use only NAND gate to implement 4

$Y = (a + b + c)(a + b + d)$

3. (a) Draw the block diagram of an Encoder. 2

(b) Design a 2 to 4 Decoder. 5

(c) Write down the truth table of a full subtractor. 3

(d) Smplify using k-map method

$f(a, b, c) = \sum m(0, 2, 3, 4, 5)$ 4

4. (a) Draw the logic circuit of S-R latch with enable and explain its function with truth table. 2+4=6

(b) Write few important differences between sequential and combinational circuits. 3

(c) Explain the truth table of J-K latch along with its logic diagram. 5

5. (a) Design a 4 : 1 Multiplexer. 5

(b) Write Ex-3 and BCD code of decimal 245. 2

(c) State commutative and distributive law of Boolean algebra. 3

(d) Write a 3 bit gray code sequence. 2

(e) Draw the block diagram of 1 : 8 demultiplexer. 2

6. (a) Design a Full Adder. 5

(b) Use only NOR gate to implement complementary, AND, OR functions. 6

(c) Convert the following into cannonical form. $f(x, y, z) = x' + yz$. 3

7. (a) Draw the block diagram of 2 bit ripple carry adder. 2

(b) Draw the block diagram and describe the operation of a 2 bit binary counter. 6

(c) Describe the operation of a 3 bit Register with its block diagram. 6