Total No. of printed pages = 8

END SEMESTER EXAMINATION–2021

Subject Code : CAI-505

MICROPROCESSORS AND APPLICATIONS

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Instructions :

(i) *All* questions of PART–A are compulsory.

(ii) Answer any *five* questions from PART–B.

PART–A

Marks–25

1. Choose the correct answer. 1×5=5

   (a) Which general register or general register pair is incremented/decremented by 2 during PUSH and POP instructions ?

   (i) H-L (ii) D-E

   (iii) Stack Pointer (iv) Program Counter

[Turn over

(b) XCHG instruction exchanges the content of H-L with _____ register pair.

(i) B-C (ii) PSW

(iii) D-E (iv) Stack Pointer

(c) _____ is used to read the status of the hardware interrupts (RST 7.5, RST 6.5, RST 5.5) by loading into the A register a byte which defines the condition of the mask bits for the interrupts.

(i) SIM (ii) RIM

(iii) DI (iv) EI

(d) During which T-state, contents of OP code from memory are loaded into IR (Instruction Register) ?

(i) T1 OP code fetch

(ii) T2 OP code fetch

(iii) T3 OP code fetch

(iv) T4 OP code fetch

(e) CALL instruction is a ——— instruction.

(i) 4 bytes (ii) 2 bytes

(iii) 1 byte (iv) 3 bytes

2. Fill in the blanks : 1×10=10

(i) The instruction SUB A will make the contents of accumulator ———.

(ii) ——— bits are used in the data bus for 8085.

(iii) Because microprocessor do not understand mnemonics as they are, they have to be converted to ———.

(iv) 8085 has ——— numbers of flag.

(v) An Instruction has two parts: Opcode and the ———.

(vi) The address bus width of 64 KB of memory is ———.

(vii) ——— machine cycles are needed for execution of 1 byte instruction.

(viii) ——— numbers of T-states are required for execution of OUT 80H instruction.

(ix) ——— instruction rotates the content of accumulator one bit right along with carry.

(x) JNC is a conditional ——— instruction.

3. Write true or false : 1×10=10

(i) Program counter is part of memory.

(ii) READY signal is used to provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.

(iii) In 8085 microprocessor, data-bus and address bus are multiplexed in order to reduce the number of pins.

(iv) In intel 8085A microprocessor ALE signal is made high to enable the data bus to be used as low order address bus.

(v) The frequency of the driving network connected between pins 1 and 2 of 8085 microprocessor is twice the desired frequency.

(vi) B-C register pair used to indicate memory.

(vii) Assembly language is independent of microprocessors.

(viii) The term "Memory Map" is used to for entire address range of a memory chip.

(ix) TRAP has the highest priority out of all the interrupts of 8085.

(x) Tristate device has the two states: low and high.

PART – B

Marks – 45

4. (a) Identify the m/c cycles of the instructions: SUB B; ADI 12H. 2

   (b) How does a microprocessor differentiate between an Opcode and data ? 2

   (c) State the functions of the signals: ALE, IO/M. 2

   (d) Assemble the following program starting with memory address C296H and specify the total number of bytes consumed 3

   MVI C, 86H

   MVI A, F2H

   ADD C

   ORA A

   STA D100H

   HLT

5. (a) If the clock frequency is 5MHz, how much time is required to execute instruction of 18 T-states ? 2

(b) If the size of a memory chip is 1024 × 4 bits, how many such chips will be required to make up 16 kilobytes of memory? 1

(c) Name the machine control instructions of 8085. 2

(d) Design a 8-bit register (8 input lines and 8 output lines) to store 8 bits using flip flops. 4

6. (a) For the following program given below- 4

LXI B, D000H

MVI A, F2H

ADI A7H

ORA A

INX B

STAX B

RST 1

Answer the following :

(i) What is the status of flags after the execution of the instruction ORA A ?

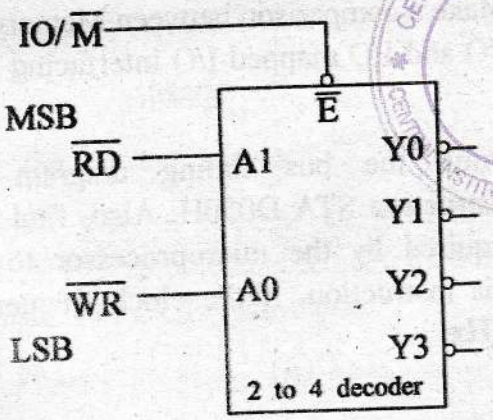
(ii) At the end of the program, what will be the content of accumulator and where will it be stored?

(b) Define the term Flag and explain how the different flags of 8085 are affected. 5

7. (a) Write an assembly language program to generate a delay of 100 msec. 5

(b) Write an assembly language program to exchange the content of Reg L with content of Reg C. Load EAH in register L and 97H in register C. Also draw the flow chart. 4

8. (a) Identify the control signals that are generated at the output of the 2 to 4 decoder as shown below : 4



(b) Write an Assembly language program for 8085 microprocessor to exchange the contents of memory block D000 H-D004 H with that of E000 H-E004 H. 5

9. Calculate the COUNT to obtain a 100μSec loop delay and express the value in Hex. 9

	T-States
MVI B, COUNT	4
LOOP: MOV A, B	4
NOP	4
DCR A	4
JNZ LOOP	10/7

10. (a) Make a comparison between Memory mapped I/O and I/O mapped I/O interfacing schemes. 4

(b) Draw the bus timing diagram of the instruction STA D050H. Also, find the time required by the microprocessor to execute this instruction, if the clock frequency is 5 MHz. 5