RE-TEST EXAMINATION, 2020

Semester: 3rd

Subject code: CAI-303

Subject: DIGITAL CIRCUITS

Full Marks: = 70 (part A- 25 + Part B- 45)

Duration: 3 hours

Instructions:

1. Questions on Part A are compulsory
2. Answer any five questions from Part B

PART-A MARK-25		
Questions no.	Questions	marks
Question No.1	Fill in the blanks:	1x10=10
1a	The binary number that come immediately after $(10111)_2$ is	
1b	The octal number that come immediately after $(177)_8$ is	
1c	The hexadecimal equivalent of $(1011001111)_2$ is	
1d	BCD equivalent of decimal number $(214)_{10}$ is	
1e	..... gate is also called as inverter.	
1f	NAND and NOR are called as	
1g	A full-adder has ..... number of inputs.	
1h	The number of input lines of a Decoder with "n" output lines is	
1i	Number of full-adders required to build a 4-bit binary adder is	
1j	"D" in D-flip-flop stands for	
Question No.2	Write true or false:	1x10=10
2a	The Gray code equivalent of $(1101)_2$ is 1001.	
2b	The binary code of letter "B" in ASCII code is $(01000001)_2$.	
2c	Adding 1's complement of a binary number X to another binary number Y yields Y-X.	
2d	The output of Ex-OR gate is HIGH when both inputs are similar.	
2e	Ex-OR gate can be used to implement a NOT gate.	
2f	A half-adder and a half-subtractor requires same number of gates.	
2g	In Boolean Algebra, X.X.X=X.	
2h	In a 3-variable Boolean Expression, a group of four 1's in the corresponding K-Map will yield a term having 3 literals.	
2i	D-flip-flop can be constructed using J-K flip-flop.	
2j	A modulo-10 counter needs 4-flip-flops.	
Question No. 3	Choose the correct answer	1x5=5
Q 3a	Binary equivalent of Gray code 110011 is-	
i) 100111	ii) 100010	
iii) 101010	iv) 100100	
3b	$(77)_8 + (01)_8$ is	

i)	$(80)_8$	ii) $(100)_8$	
ii)	$(10A)_8$	iv) None of these.	
3c	One of the inputs of a two-input NAND gate is permanently tied to logic '1. The output will be-		
i)	0	ii) independent of other input	
iii)	dependent on other input	iv) at HIGH impedance	
3d	The complement of the expression $(A + B)$ is -		
i)	$(A.B)$	ii) $\overline{A.B}$	
iii)	$(\bar{A}.\bar{B})$	iv) None.	
3e	A multiplexer has "m" select lines and "n" input lines, then-		
i)	$n=2^m$	ii) m=n	
iii)	$m=2^n$	iv) None of these.	

PART-B, MARK-		
Questions No.	Questions	marks
Question No. 4		
Q4a	Perform the following operations using 8-bit 2's complement arithmetic- i. $(30)_{10} - (20)_{10}$ ii. $(09)_{10} - (24)_{10}$	4
Q4b	Perform BCD addition- i. $(125)_{10} + (216)_{10}$ ii. $(654)_{10} + (275)_{10}$	4
Q4c	What is Excess-3 code?	1
Question No.5		
Q5a	Minimize using Boolean Algebra theorems- i. $A.\bar{B}.\bar{C} + \bar{A}.B.C + A.B.C + A.\bar{C}$ ii. $(A + \bar{B} + C).(A + B + C).(A + B + C).(\bar{A} + B + C)$	4
Q5b	Minimize using K-map technique. $F(A,B,C,D) = \sum m(0,1,2,3,8,9,10,11) + \phi(7)$	5
Question No. 6		
Q6a	A digital circuit has four input lines and output lines, such that the output goes LOW whenever two or more input lines get HIGH inputs. Determine the truth table, simplified output expression and draw the logic circuit using basic gates.	9
Question No. 7		
Q7a	Explain the working of a full subtractor circuit with the help of its truth table and logic diagram.	6
Q7b	Design a full-adder circuit using two half-adders.	3
Question No. 8		
Q8a	Design and explain the working of a 3-bit parallel binary adder.	9
Question No. 9		
Q9a	Implement the Boolean function $F(A, B) = \sum(1,2)$ with a 4:1 MUX.	4

Q9b	Draw the block diagram of a 2-to-4 line decoder and draw its truth table.	5
Question No. 10.		
Q10a	Differentiate between Combinational and Sequential Circuits.	2
Q10b	Draw the logic diagram of a J-K flip-flop with NAND gates and write its characteristic table.	7
Question No. 11	Explain the working of a master-slave J-K flip-flop.	9