END SEMESTER/ RE-TEST EXAMINATION, 2020

Semester: 5th

Course Code: CAI-505

Course Title: Microprocessors and Applications

Full Marks: 70

Time: 3 Hours

The Question Paper consists of two parts: Part-A and Part-B. Both are compulsory.

Part-A (Marks = 25)

All questions are compulsory

1. Choose the correct answer.

a) What is mean by ALU

i) Arithmetic logic upgrade

ii) Arithmetic logic unsigned

iii) Arithmetic local unsigned

iv) Arithmetic logic unit

b) 8085 microprocessor has how many pins

i) 30.

ii) 39.

iii) 40.

iv) 41.

c) In 8085 microprocessor, the RST6 instruction transfer program execution to following location

i) 0030H.

ii) 0024H.

iii) 0048H.

iv) 0060H.

d) HLT opcode means

i) load data to accumulator.

ii) store result in memory.

iii) load accumulator with contents of register.

iv) end of program.

e) In 8085 name/names of the 16 bit registers is/are

i) stack pointer.

ii) program counter.

iii) both A and B.

iv) none of these.

f) What is SIM?

i) Select interrupt mask.

ii) Sorting interrupt mask.

iii) Set interrupt mask.

iv) None of these.

g) In 8085 microprocessor ALE signal is made high to

i) Enable the data bus to be used as low order address bus

ii) To latch data D0-D7 from data bus

iii) To disable data bus

iv) To achieve all the functions listed above

h) The processor status word of 8085 microprocessor has five flags namely:

i) S, Z, AC, P, CY

ii) S, OV, AC, P, CY

iii) S, Z, OV, P, CY

iv) S, Z, AC, P, OV

i) In 8085, which is the first machine cycle of an instruction?

i) An op-code fetch cycle

ii) A memory read cycle

iii) A memory write cycle

iv) An I/O read cycle

j) In 8085 microprocessor, why is READY signal used?

i) To indicate to user that the microprocessor is working and is ready for use.

ii) To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.

iii) To slow down a fast peripheral device so as to communicate at the microprocessor's device.

iv) None of the above.

k) The output data lines of microprocessor and memories are usually tristated because

i) More than one device can transmit information over the data bus by enabling only one device at a time

ii) More than one device can transmit over the data bus at the same time

iii) The data line can be multiplexed for both input and output

iv) It increases the speed of data transfer over the data bus

l) When referring to instruction words, a mnemonic is

i) a short abbreviation for the operand address.

ii) a short abbreviation for the operation to be performed.

iii) a short abbreviation for the data word stored at the operand address.

iv) shorthand for machine language.

m) In 8085 microprocessor system with memory mapped I/O, which of the following is true?

i) Devices have 8-bit address line

ii) Devices are accessed using IN and OUT instructions

iii) There can be maximum of 256 input devices and 256 output devices

iv) Arithmetic and logic operations can be directly performed with the I/O data

n) In a microcomputer , the address of memory locations are binary numbers that identify each memory circuit where a byte is stored. If a microcomputer uses 20-bit address, then numbers of different memory locations are

i) 20

ii) 220

iii) 220-1

iv) 220 - 1

o) Number of Hex digits needed to represent the 20-bit address of a memory location are

i) 20

ii) 16

iii) 5

iv) 4

2. Fill in the blanks

i) A group of 4 bits is called .....

ii) ASCII s a 7 bit alphanumeric code with.....combinations.

iii) The instruction ADD A will make the accumulator content.....

iv) ..... bytes make a word of 32 bits.

v) .....address lines are required to address 32 KB memory.

3. Write true or false:

i) Accumulator is a 16 bit register of 8085.

ii) HLT and JMP are machine control instructions

iii) ALU performs arithmetic and logic operations.

iv) STA E000H is a two byte instruction.

v) Parity flag is set when the result of an arithmetic or logical operation has oddno's of 1's.

Part-B (Marks = 45)

Answer any five (5) questions

4. (a) Why is 8085 called an 8-bit microprocessor? **(1)**

(b) How does a microprocessor differentiate between an Opcode and data? **(2)**

(c) Specify the opcode, operand and meaning of the following instructions- **(2)**

i) MVI 25H ii) LXI HF000H

(d) Assemble the following program starting with memory address B1FFH and specify the total number of bytes consumed- **(4)**

MVI B, 56H

MVI A, 92H

ADD B

ORA A

STA F23EH

HLT

5. (a) If the size of a memory chip is 1024 X 8 bits, how many such chips will be required to make up 64 Kbytes of memory? **(1)**

(b) Specify the status of Carry and Zero flags when following instructions are executed. Assume that the content of the Accumulator is FFH. **(8)**

i) ADD A ii) MVI A, 00H iii) ORA A iv) DCR A

6. (a) Write an Assembly language program for 8085 microprocessor to exchange the contents of memory block D000 H-D004 H with that of E000 H-E004 H. **(4)**

(b) Define the term Flagand explain how the different flags of 8085 are affected. **(5)**

7. (a)Design a 4-bit register (4 input lines and 4 output lines) to store 4 bits using latches/flip flops. **(4)**

(b) Write an assembly language program to exchange the content of Reg H with content of Reg D. Load 9AH in register H and F7H in register D. Also draw the flow chart. **(4)**

(c) The starting memory address of a 4K byte memory chip is given as E000H. Specify the last memory address of the chip. **(1)**

8. (a) What is the function of accumulator? **(2)**

(b) Identify the m/c cycles of the instructions: SUB B; ADI 12H **(2)**

(c) Calculate the number of registers in a 64K memory board. **(2)**

(d) State the functions of the signals: ALE, IO/$\overline{M}$. **(2)**

(e) If the clock frequency is 5MHz, how much time is required to execute instruction of 18 T-states? **(1)**

9. Calculate the COUNT to obtain a 100μSec loop delay and express the value in Hex. **(9)**

	T-States
MVI D, COUNT	4
LOOP: MOV A, D4	
NOP	4
NOP	4
JNZ LOOP	10/7

10.(a) Make a comparison between Memory mapped I/O and I/O mapped I/O interfacing schemes. **(4)**

(b) Draw the timing diagram of LDA, D255H instruction. **(5)**

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