53 (IT 303) DGLD

2019

DIGITAL LOGIC DESIGN

Paper : IT 303 (Back)

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following : 1×3=3

   (i) $(51)_8 = (\ )_2$

   (ii) $(AB1)_{16} = (\ )_2$

   (iii) $(17.75)_{10} = (\ )_2$

   (b) Draw the symbol of a *X*-OR gate and write down the truth table of the same. 2

(c) Convert $Y = (a+b)c$ into Canonical POS form. 2

(d) Prove that $(a+bc) = (a+b)(a+c)$ 3

(e) Describe the function of a 4:2 Encoder with truth table, block diagram, logic diagram. 5

(f) Convert the following: 1×2=2

(i) $(412)_{10} = (\ )_{16}$

(ii) $(412)_{10} = (\ )_{8}$

(g) Simplify : $Y = \overline{abc} + \overline{a}\,\overline{b}\,\overline{c} + abc + \overline{\overline{a}\,b\overline{c}}$ 3

2. (a) Define Minterm and explain with an example. 1+2=3

(b) Simplify :

$Y = \sum m(0,2,4,9,10,11,12,13,14) + d(1)$

using K – map method. 6

(c) Describe S–R Latch with logic diagram, truth table. 5

(d) Describe a 1:4 De-multiplexer. 5

(e) How many control lines are needed to design a 32:1 Multiplexer ? 1

3. (a) Describe 3-bit asynchronous counter with block diagram, timing diagram and necessary table. 7

(b) Design a Mod-7 counter with J-K flip flop. 13

4. (a) Draw the state transition diagram of a S-R flip flop. 3

(b) Derive the characteristics equations of a S-R flip flop. 3

(c) Simplify :

$Y = \overline{x}\,y\,\overline{z} + \overline{xy+z} + (\overline{x}+\overline{y})(x+xyz)$

using Boolean algebraic techniques. 3

(d) Simplify : $Y = \Pi M(0,2,3,4,5,6,7,8)$ into POS form using K-map method. 6

(e) Describe the function of a 3-bit Ripple Carry Adder with block diagram. 4

(f) Find out the 1's Complement of 101011. 1

5. *(a)* Design a full adder using minimum basic logic gates. 5

(b) Explain the operation of a pulse triggered SR latch. 4

(c) Describe the function of a Master slave D flip flop. 4

(d) State commutative law of Boolean algebra. 2

(e) Draw the logic diagram of 1-bit comparator. 2

(f) Use basic gates to realize $Y = \overline{\bar{a}\,\bar{b}\,\bar{c}\,\overline{(abc)}} + ab\bar{c}$ without simplifying the equation. 3

6. *(a)* Design MOD-5 counter using D-flip flop. 7

(b) Use only NAND gate to implement $Y = a\bar{b} + c$. 3

(c) Use only NOR gate to implement $Y = (a+b)(c+d)$. 3

(d) Draw the logic diagram of a D-latch. 2

(e) Describe the function of a odd parity generator and checker. 5

7. *(a)* *(i)* BCD code of 91 = _____.

(ii) $x + \bar{x} + 1 =$ _____.

(iii) $1 \oplus 1 \oplus 1 \oplus 1 \oplus 1 =$ _____.

(iv) $a + \bar{a}c =$ _____.

(v) Ex-3 code of a1 = _____. 1×5=5

(b) Explain the truth table of J-K latch. 4

(c) Write down the truth table of a full subtractor. 3

(d) Distinguish between combinational logic and sequential logic. 2

(e) Use basic logic gates to implement $Y = (x+y)\overline{xy} + \bar{x}\bar{y}z + x\overline{yz}$ 3

(f) Write down the logic diagram of a 4:1, Multiplexer using basic gates. 3