53 (EC 401) DGED

2019

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Explain the working of a basic RTL inverter and draw the transfer characteristics clearly specifying the various parameters involved. 6

(b) Define the following characteristic parameters for logic families : V_{IH}, V_{OH}, Fan-out and Noise Margin. 4

(c) Draw the circuit diagram of an Open Collector Gate TTL for NAND operation. 4

Contd.

(d) Implement OR and AND gates using CMOS logic. 6

2. (a) Perform BCD arithmetic operations for the following : 4

(i) $(458)_{10} + (386)_{10}$

(ii) $(789)_{10} + (295)_{10}$

(b) For the Boolean function $Y(A, B, C) = \Sigma m(0, 4, 5, 6)$, write the o/p expression in terms of SOP and POS, minimize the expressions and implement *any one* of the two expressions using basic gates. 6

(c) A digital circuit has three i/p lines and two o/p lines such that the o/p bits are binary equivalent of the number of '1's present at the i/p lines. Find out the truth table and draw the logic circuit with least number of gates. 6

(d) Simplify using *K*-map technique.

$Y(A, B, C, D) = \Sigma m(1, 5, 6, 7, 10, 12, 13) + \phi(4, 14)$ 4

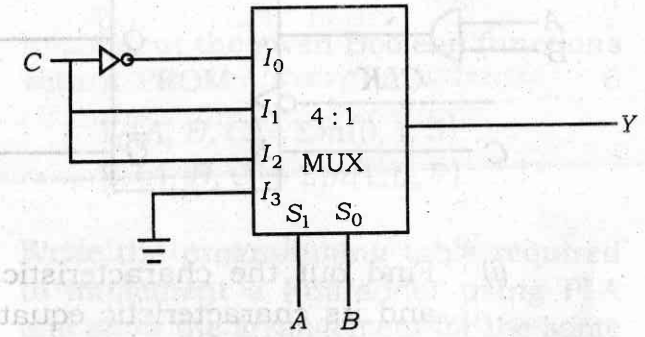
3. (a) Explain the working of a full subtractor with the help of its truth table and logic circuit. 5

(b) How many Half-adders will be required to add two 3-bit data ? Show and explain the arrangement with block diagrams. 1+5=6

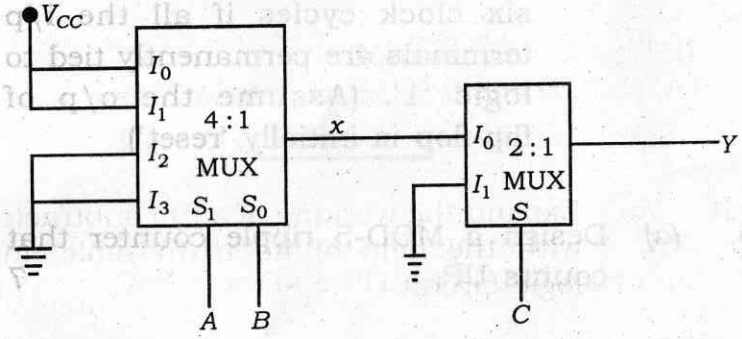
(c) Implement a Full-adder using a 3-to-8 line Decoder and few additional gates. 4

(d) For the arrangement given below, find the o/p expressions. 2+3=5

(i)



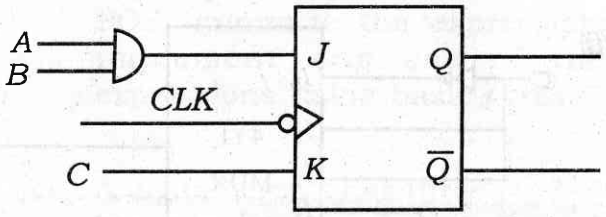
(ii)



4. *(a)* Explain the working of Active HIGH J-K flip-flop with the help of its characteristic table and logic circuit using NAND gates. 5

(b) Design a D-flip-flop with the help of J-K flip-flop. 5

(c) For the flip-flop given below, answer the following questions : 4+6=10



(i) Find out the characteristic table and its characteristic equation.

(ii) Show the o/p waveform for at least six clock cycles if all the i/p terminals are permanently tied to logic '1'. (Assume the o/p of flip-flop is initially 'reset')

5. *(a)* Design a MOD-5 ripple counter that counts UP. 7

(b) Design a synchronous counter that has the following sequence — 8

$0 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 0$

(c) Explain how D-Latches can be used to construct a 4-bit register for storage of data. 5

6. *(a)* Draw the circuit diagram of static RAM and explain its principle of operation. 6

(b) Implement the given Boolean functions with a PROM 6

$Y_1(A, B, C) = \Sigma m(0, 1, 5)$

$Y_2(A, B, C) = \Sigma m(1, 6, 7)$

(c) Write the programming table required to implement a Full-adder using PLA and show the arrangement for the same using a suitable PLA. 8