Total No. of printed pages = 7

END SEMESTER EXAMINATION, NOVEMBER-2018

Semester : 3rd (New Syllabus)

Subject Code : CO-303

COMPUTER ARCHITECTURE AND ORGANIZATION

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Instructions :

1. *All* the questions of PART-A are compulsory.
2. Answer any *five* questions from PART-B.

PART – A

Marks – 25

1. Fill in the blanks : 1×10=10

   (a) 4 to 1 MUX(Multiplexer) would have ——— output.

   (b) The characteristic of J-K flip-flop is similar to ———.

[Turn over

(c) ——— is a universal logic gate.

(d) The Full form of DR is ———.

(e) The last on the memory hierarchy devices is ———.

(f) EEPROM stands for ———.

(g) The two major types of control organization are hardwired control and ———.

(h) The most efficient method followed by computers to multiply two signed numbers is by using ——— algorithm.

(i) The term used to define all input and output devices in a computer system is ———.

(j) The process where in the processor constantly checks the status flags is called as ———.

2. Write true or false : 1×10=10

(a) Demultiplexer converts single input into multiple outputs .

(b) An encoder is called as multiplexer.

(c) The decimal numbers represented in the computer are called as floating point numbers, as the decimal point floats through the number.

(d) The usual BUS structure used to connect the I/O devices is Star BUS structure.

(e) The registers used to store the flags are called as Status registers.

(f) The addressing mode, where you directly specify the operand value is Immediate Addressing.

(g) To reduce the memory access time we generally make use of secondary memory.

(h) Virtual memory is generally used to increase the apparent size of physical memory.

(i) Interpreter is an example of hardware.

(j) In memory-mapped I/O, the I/O devices have a seperate address space.

3. Choose the correct answer : 1×5=5

(a) The first computers were programmed using

(i) assembly language

(ii) machine language

(iii) source code

(iv) object code

(b) —— is used to store data in registers.

(i) D fip flop

(ii) JK flip flop

(iii) RS flip flop

(iv) None of the mentioned above

(c) Which of the following is a part of the Central Processing Unit ?

(i) Printer

(ii) Keyboard

(iii) Mouse

(iv) Arithmetic and logic unit

(d) The fastest data access is provided using

(i) Caches (ii) DRAM's

(iii) SRAM's (iv) Registers

(e) What does DMA stand for ?

(i) Distinct Memory Access

(ii) Direct Memory Access

(iii) Direct Module Access

(iv) Direct Memory Allocation

PART – B

Marks – 45

4. (a) Write briefly about Von-Neumann architecture. 3

(b) Write truth tables for the following Logic gates :

(i) NAND (ii) NOR 3

(c) Draw the logic circuit of the following : 3

(i) AB +BC + ABC

(ii) (X+Y)(Y+Z)(Z+X)

5. (a) Draw the logic diagram of half adder and full adder and explain with the help of truth table. 4

(b) What do you mean by signed number representation by computer system. 3

(c) Find the 2's complement form of the number 1010111. 2

6. (a) What are computer registers ? Name them and write their purposes. 3

(b) Define addressing modes. What are direct and indirect addressing ? 3

(c) Write briefly about memory reference instructions. 3

7. (a) What do you mean by one byte instruction and zero byte instruction ? 3

(b) Write briefly about stack organization. 3

(c) Write briefly about microprogrammed control unit. 3

8. (a) Differentiate ROM and PROM. 3

(b) What do you mean by Memory Hierarchy ? Explain briefly about Cache memory. 6

9. (a) Differentiate between memory mapped I/O and isolated I/O. 4

(b) Write brief note on any two input devices. 5

10. Explain Booth's algorithm to multiply two numbers in 2's complement form. Use the Booth's algorithm to multiply -15 decimal with -13 decimal. 9

11. Explain briefly the DMA transfer scheme. How does DMA controller works ? 9

12. Explain briefly the working principle of Virtual memory and Associative memory. 9