Total No. of printed pages = 5

END SEMESTER EXAMINATION, NOVEMBER-2018

Semester – 3rd

Subject Code : CAI–303

DIGITAL CIRCUITS

Full Marks – 70

Time – Three hours

The figures in the margin indicate full marks for the questions.

Instructions :

1. *All* questions of PART – A are compulsory.
2. Answer *all* questions from PART – B.

PART – A

Marks – 25

1. Convert the following : 1×5=5

(a) $(1100)_2 = (\_\_\_\_\_)_{10}$

(b) $(158)_{10} = (\_\_\_\_\_)_8$

(c) $(2467)_{16} = (\_\_\_\_\_)_{10}$

[Turn over

(d) $(100111100001)_2 = (\_\_\_\_\_)_{16}$

(e) $(2568)_8 = (\_\_\_\_\_)_2$

Multiple choice questions. 1×5=5

2. Choose the correct answer :

(a) $A'A =$

(i) 1 (ii) 0

(iii) A (iv) A'

(b) A D-flip-flop can store

(i) 1 bit (ii) 2 bits

(iii) 3 bits (iv) 4 bits

(c) 2's complement of 11001110 is

(i) 10110001 (ii) 00110010

(iii) 11100011 (iv) 10111100

(d) Number of select lines in a 8:1 multiplexer is

(i) 2 (ii) 4

(iii) 3 (iv) 5

(e) $A'BC + AB'C =$

(i) $A + B$ (ii) B

(iii) C (iv) A

3. State whether true or false : 1×15=15

(i) Decoder is a combinational circuit.

(ii) $(xy)' = x' + y.$

(iii) Multiplexer is a data selector circuit.

(iv) Excess 3 code is an example of alpha numeric code.

(v) A register is a memory circuit.

(vi) $x + x' = 1.$

(vii) Synchronous circuit uses external clock to enable all the flip-flops.

(viii) $x + xy = x.$

(ix) 3 bit register can count upto 9.

(x) An XOR gate can be realized by 5 NAND gates.

(xi) $(x'y')' = xy$.

(xii) A full adder can add 2 bits only.

(xiii) $x + y = y + x$ is an example of commutative law.

(xiv) J-K flip-flop is a combinational circuit.

(xv) 1's complement of 1001 is 0110.

PART B

Marks 45

4. Simplify the following using Boolean algebra :

(a) $ABCD + AB'C'D + AB'CD + ABCD'$

(b) $(A + B' + C')(A + B + C)(A' + B + C)$ 3×2=6

5. Simplify using K-Map : 6×3=18

(a) $f(A, B, C, D) = \Sigma (1, 3, 4, 5, 6, 9, 11, 12, 15)$

(b) $f(W, X, Y, Z) = \Sigma (0, 2, 4, 5, 7, 9, 10, 13, 15)$

(c) $f(A, B, C, D) = \Sigma (0, 2, 3, 4, 6, 8, 11, 12, 14)$

6. Implement the following using NAND gates only : 6×2=12

(a) Half adder

(b) 2×4 Decoder

7. Write short notes on : 3×3=9

(a) J-K Flip-flop

(b) Universal gate

(c) 3-bit Register.