53 (EC 602) VLSI

2018

VLSI

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer ***any four*** *questions from Q. Nos.* ***1–5*** *and Q.* ***6*** *is* ***compulsory.***

1. *(a)* Describe the operation of nMOS and PMOS as pass transistors. 5+5

(b) Mention the different types of parasitic capacitances in a MOS transistor under different operating modes. 5

(c) A MOSFET can operate as a voltage controlled resistor in triode region. Explain. 5

2. (a) Implement a Full Adder using CMOS logic. 10

(b) Derive the expression for the rise time of a CMOS inverter. 5

(c) Describe the noise margin of an inverter and its effect on a cascaded inverting sections. 5

3. (a) Draw the layout of a 2 input NAND gate in CMOS technology with substrate contacts and well contacts. 5

(b) Describe the operation of (4×4) bit NAND based ROM array with proper circuit diagram. 5

(c) Write the masking steps required in an n-well CMOS technology with diagrams. 10

4. (a) Implement a Boolean function $f(A, B, C, D) = (A + B) \cdot (C + D)$ using CMOS logic. 5

(b) Give a detailed comparison between 1-bit SRAM cell and 1-bit DRAM cell. 5

(c) Implement a 4 : 1 MUX using nMOS transistor only. 5

(d) Write a short note on constant voltage scaling. 5

5. (a) Discuss the merits and demerits of a BiCMOS inverter in comparison to a CMOS inverter and hence explain the operation of a BiCMOS inverter. 3+7

(b) Describe the 4-bit rotate left operation and draw its MOS implementation. 5

(c) Describe the operation of 1-bit DRAM Cell. 5

6. 10×2=20

(a) Draw the circuit diagram of inverters in Bipolar and nMOS technology.

(b) What do you mean by a photoresist material?

(c) If oxide thickness decreases by 50%, what will happen to gate capacitance in saturation mode?

(d) What do you mean by fringe capacitance?

(e) Delay time of an inverter (CMOS) is dependent upon which parameters of MOSFET?

(f) Why design rules are necessary? Mention the types of design rules.

(g) What do you mean by channel length modulation?

(h) Mention different types of integrated resistors in CMOS technology.

(i) What happens to the intrinsic delay parameter due to the effect of Constant Field Scaling?

(j) If V_{SB} increases, what will happen to the threshold voltage of an nMOS transistor?
