53 (EC 401) DGEL

2018

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer **any five** questions.

1. *(a)* Differentiate between : 4

    (i) Analog and Digital signal

    (ii) +ve and –ve logic system.

    (b) Using 8-bit 2's complement arithmetic, perform the following operations —

    (i) (+ 42) – (+ 12)

    (ii) (– 24) – (+12) 4

(c) Convert the following BCD codes into its equivalent Binary and Gray codes :

(i) $(0110 \ 0100)_{BCD}$

(ii) $(0011 \ 0010)_{BCD}$

4

(d) Implement OR and Ex-OR using only NAND gates. 4

(e) Draw the logic diagram and find the truth table for the expression given below —

$$Y = (A+B)\overline{C} + AB$$

4

2. (a) Reduce the following Boolean expression — 4

(i) $AB + A(B+C) + \overline{B}(B+D)$

(ii) $\overline{B}\,\overline{C}D + (\overline{B+C+D}) + \overline{B}\,\overline{C}\,\overline{D}E$

(b) Simplify using K-map and find the reduced Boolean expression —

6+4=10

(i) $F = \Sigma m(0, 1, 8, 9, 12, 13, 16, 17, 29) + d(28)$

(ii) $Y = \pi m(1, 7, 10, 11, 14, 15)$

(c) A digital circuit accepts a 4-bit data and generates a HIGH output bit whenever the number of 1's in the input data is zero or the data is an invalid BCD. Find the truth table and draw the simplified logic circuit using basic gates. 6

3. (a) Explain the working of a full-adder.

4

(b) Show the arrangement for performing subtraction using 2's complement with the help of 4-bit binary adder and few additional gates. 6

(c) Design a 4-bit binary to BCD code converter. 10

4. (a) Briefly describe the following terms for any logic device — 8

Propagation Delay, Power dissipation, Fan-out and Noise margin.

(b) Realize the following Boolean Expression using 8 : 1 MUX.

$$Y = \Sigma m(1, 4, 7, 12, 14, 15).$$

6

(c) Implement a Full-subtractor using a 3-to-8 Decoder. 6

5. (a) Design a BCD to XS-3 code converter using PLA. 16
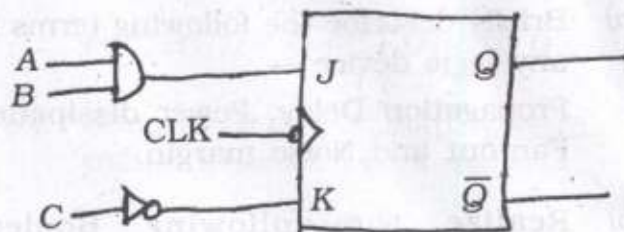
(b) Explain the working of an Active HIGH S-R Latch. 4

6. (a) Write the characteristic table of the following flip-flops and derive the transition tables : 6

(i) J-K flip-flop

(ii) T flip-flop.

(b) For the flip-flop given below, answer the questions that follow :
2+2+4=8

(i) Find the characteristic table in terms of A, B and C inputs.

(ii) Characterisitc equation in terms of A, B, C.

(iii) Assuming that all the i/ps A, B, C are HIGH initially, show the o/p waveform when 'C' gets a LOW input at 2nd clock pulse.

(c) Convert a J-K flip-flop to D flip-flop. 6

7. (a) Design a BCD Decode Counter. 6

(b) Design a synchronous counter that has the following sequence —
$$0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 0$$
8

(c) Explain the working of a SISO Shift Register. 6

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