53 (IT 303) DLDG

2018

DIGITAL LOGIC DESIGN

Paper : IT 303

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following : 1×3=3

   (i) $(41)_8 = (\ )_2$

   (ii) $(DF2)_{16} = (\ )_2$

   (iii) $(12{\cdot}25)_{10} = (\ )_2$

   (b) What do you understand by binary coding ? Explain with an example. 3

(c) State De Morgan's theorem of Boolean Algebra. 2

(d) Simplify $Y = \overline{abc} + abc + \bar{a} + \bar{a}bc$ using Boolean algebraic techniques. 2

(e) Draw the symbol of an X-NOR gate and write down the truth table of the same. 2

(f) Describe the function of a 4:2 Encoder with truth table, block diagram, logic diagram. 5

(g) Convert $Y = ab + c$ into Canonical SOP form. 3

2. (a) Define Maxterm and explain with an example. 3

(b) Simplify

$Y = \sum m(0, 1, 3, 5, 9, 10, 11, 12, 14) + d(2, 13)$

using K-map method. 6

(c) Describe JK latch with logic diagram, truth table. 5

(d) Design a 1:8 De-multiplexer. 5

(e) How many control lines are needed to design a 16:1 Multiplexer. 1

3. (a) Describe 4-bit asynchronous counter with block diagram, timing diagram and ncessary table. 7

(b) Design a Mod–5 Counter with JK flip-flop. 11

(c) Distinguish between truth table and transition table. 2

4. (a) Draw the State Transition diagram of a JK flip-flop. 3

(b) Derive the characteristic equations of a JK flip-flop. 3

(c) Simplify

$Y = x\bar{y}z + \overline{xy + z} + (x + \bar{y})(x + yz) + xz$

using Boolean algebraic techniques. 3

(d) Simplify

$Y = \Pi M(0, 1, 3, 4, 5, 9, 10, 11, 12)$ into POS form using K–map method. 6

(e) Describe the function of a 4-bit Ripple Carry Adder with block diagram. 4

(f) Find out the 2's complement of 111001111. 1

5. (a) Design a Full subtractor using minimum basic logic gates. 6

(b) Explain the operation of a pulse-triggered SR latch. 4

(c) Draw the block diagram of a Negative-edge triggered master-slave JK flip-flop. 2

(d) Draw the State Transition diagram of a SR flip-flop. 2

(e) State Distributive Law of Boolean Algebra. 2

(f) Draw the block diagram of a 3-bit synchronous counter using JK flip-flop. 2

(g) Draw the block diagram of a 3-bit Register using D flip-flop. 2

6. (a) Design a Mod–7 Counter using D flip-flop. 10

(b) Convert the following : 2

(i) $(F12)_{16} = (\ )_2$

(ii) $(1101{\cdot}01)_2 = (\ )_{10}$.

(c) Use only NOR gate to implement $Y = ab + c$. 3

(d) Use only NAND gate to implement $Y = \bar{a}b + c$. 3

(e) Derive the characteristic equations of a D flip-flop. 2

7. (a) Use basic logic gates to implement $Y = \overline{ab} + ab\overline{cd} + a\bar{b}c + \overline{abc}\,d$. 3

(b) State Commutative Law of Boolean Algebra. 1

(c) Draw the logic diagram of a 1-bit comparator. 2

(d) Distinguish between combinational and sequential logic. 2

(e) Prove that $\overline{a + b + c} = \bar{a} \cdot \bar{b} \cdot \bar{c}$. 2

(f) Draw the logic diagram of a D latch. 2

(g) Draw the block diagram of a 8:1 multiplexer. 1

(h) Draw the symbol of a Positive-edge triggered, master-slave flip-flop. 1

(i) Prove that $x + \bar{x}y + \bar{x}yz = x + y$. 1

(j) Define Minterm. 1

(k) $1 \oplus 1 \oplus 0 \oplus 1 \oplus 0 =$ _____. 1

(l) Ex–3 code of 91 = _____. 1

(m) BCD code of 41 = _____. 1

(n) Prove that $(x + yz)(x + w\bar{x})(x + \bar{y}z) = x$. 1