53 (IT 301) COAR

2018

COMPUTER ORGANIZATION AND ARCHITECTURE

Paper : IT 301

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* What are the possible ways to represent signed numbers in computer? 7

   (b) When does the condition of overflow occur while adding two numbers in 2's complement? How can it be detected? 5

   (c) Evaluate the following floating point numbers in decimal form: 8

   (i) $(41200000)_{16}$

   (ii) $(C4962800)_{16}$

2. *(a)* Divide 19 by 4 using restoring division algorithm. 10

(b) Consider a processor with 64 registers and an instruction set of size 12. Each instruction has five distinet fields, namely opcode, two source registers, one destination register and a 12-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. What is the amount of memory (in bytes) consumed by the program, if a program has 100 instructions? 10

3. How does the instruction pipeline work? What are the various situations where an instruction pipeline can deviate from its normal operation? What can be its resolutions? 5+5+10

4. *(a)* A RAM chip has a capacity of 1024 words of 8 bits each (1*K*×8). What is the number of 2×4 decoder with enable line needed to construct a 16*K*×16 RAM from 1*K*×8 RAM?

(b) A digital computer has a memory unit of 64*K*×16 and a cache memory of 1*K* words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block and word fields of the address format?

(ii) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.

(iii) How many blocks can the cache accommodate? 10

5. *(a)* What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? 5

(b) How many characters per second can be transmitted over a 1200 baud line in each of the following modes? (Assume a character code of eight bits)

(i) Synchronous serial transmission

(ii) Asynchronous serial transmission with two stop bits

(iii) Asynchronous serial transmission with one stop bit. 5

(c) A CPU with a 20*MHz* clock is connected to a memory unit whose access time is 40*ns*. Formulate a read and write timing diagrams using a READ strobe and a WRITE strbe. Include the address in the timing diagram. 10

6. *(a)* Draw the block diagram and label all input and output terminals in the RAM. Explain the function table to specify the operation of the RAM chip. 10

(b) A set-associative cache consists of 64 lines, or slots, divided into two-line sets. The main memory contains 4*K* blocks of 128 words each. Show the format of main memory addresses. 10

7. Write short notes on : 20

(a) Memory Hierarchy

(b) Interrupt

(c) BUS

(d) RISC.