53 (EC 602) VLSI

2017

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions out of **Seven**.*

1. *(a)* Implement the Boolean function $f(A,B,C,D)=\overline{A.(B+C+D)}$ using CMOS logic ϕ draw the schmatics. 4

   (b) What do you mean by noise margin for an inverter ? Explain the importance of noise margin in an inverter. How can we maximise the noise margin for an inverter ? 1+2+2

(c) Draw the diagram of inverters in various integration technologies, describe the operation of CMOS and BiCMUS inverters. 1+10

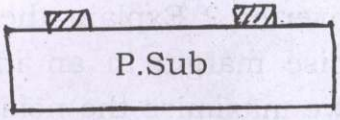
2. (a) Calculate the maximum speed of an NMOS technology. 5

(b) Draw the layout for 2 input XOR gate and 2 input XNOR gate with necessary label for the layers. 10

(c) Explain the operation of a Binary Comparator with proper logic diagram. 5

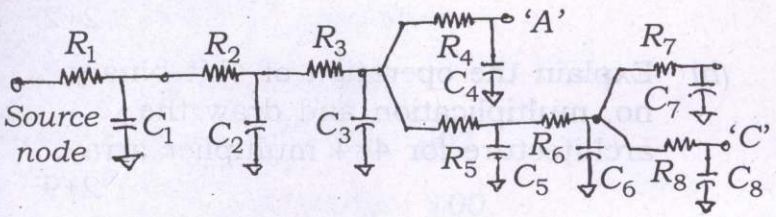
3. (a) Explain the operation of 1 bit DRAM cell, and compare the performance with 1bit SRAM cell. 6+4

(b) Describe the lithographic sequences required to pattern the oxide as shown below : 5



(c) Draw the NMOS cross-bar switch matrix for implementing 4-bit right rotation operation. 5

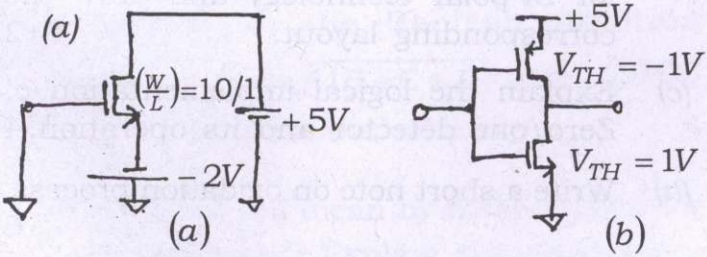
4. *(a)* Calculate the expressions for elmore's delay for the following RC-tree at *'A'*, *'B'*, *'C'*, *'D'* nodes. 10



(b) Describe the effect of constant voltage scaling on the various parameters for digital systems. 5

(c) Write a short note on the Ion implantation process. 5

5. *(a)*



(i) Calculate the drain-to-source current for the biased NMOS transistor implemented in a technology having

$\mu_n C_{ox} = 100 \mu A/v^2$ and $V_{TH_m} = +1V$

and $V_A = +40V$ fig (a).

(ii) Find the operating modes of NMOS and PMOS of an inverter if V_{in} =0·5V and V_{out} is 4·5V. 2+2

(b) Explain the operation of 4bit binary no. multiplication and draw the architecture for 4×4 multiplier array. 2+9

(c) Calculate the rise time for an inverter (CMOS). 5

6. (a) Draw the CMOS schematic of a full-Adder. 6

(b) Describe the fabrication process steps for Bi-polar technology and draw the corresponding layout. 8+2

(c) Explain the logical implementation of Zero/one detector and its operation. 4

7. (a) Write a short note on oxidation process. 6

(b) Explain the operation and architecture of NOR based ROM. 8

(c) Describe the internal parasitics of a MOS transistor and draw the high frequency modes of an NMOS transistor in saturation mode. 4+2