53 (EC 602) VLSI

2016

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

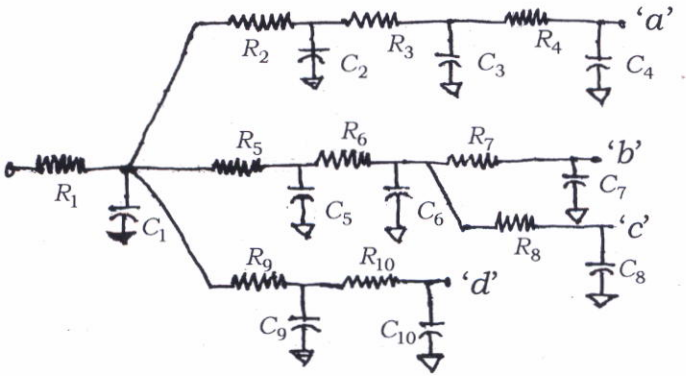
Answer ***any five*** *questions out of* ***seven.***

1. *(a)* Implement the following Boolean function is CMOS :

$$f(A,B,C,D)=\overline{(A\cdot B+C\cdot D)}$$

and draw its complete layout. 2+8

(b) Calculate the Elmore's delay for the RC tree below,



at nodes : *a, b, c, d*

2½+2½+2½+2½

2. (a) Write a short note on Ion-implantation of diffusion process. 4+3

(b) Consider an N-MOS transfer having aspect ratio $\left(\frac{8\mu m}{0{\cdot}5\,\mu m}\right)$ is made in a process having $\mu_n C'ox = 180\,\mu A/V^2$, $V_{TH} = 0{\cdot}7V$ and calculate the on resistance of MOSFET ; if $V_{DD} = 3V$, gate is connected to a battery of $4V$ and source is at ground. 3

(c) Describe the blocks of a 4-bit MPU and its function with neat diagrams. 10

3. (a) Consider a CMOS process having following parameters :

$\mu_n C'ox = 150\,\mu A/V^2$, $V_{TH,n} = 0{\cdot}8V$

$\mu_p C'ox = 70\,\mu A/V^2$, $V_{TH,p} = -0{\cdot}8V$

Calculate the switching threshold for an inverter designed in the CMOS process : where aspect ratio of N-MOS and P-MOS are $\left(\frac{20\mu m}{1\mu m}\right)$ and $\left(\frac{10\mu m}{1\mu m}\right)$ respectively and the supply voltage used is $+3V$. 4

(b) Prove that the transition frequency of a N-MOS transistor in saturation is directly proportional to transconductance and inversely proportional to gate capacitance. 6

(c) Draw the circuit diagram of an inverter in various different integration technologies and describe the fabrication process steps for an N-MOS technology. 3+7

4. (a) Implement an SR-latch (using NAND gate) in CMOS logic and draw the layout for the same circuit. 4+6

(b) Describe the importance of Noise Margin while cascading inverters. 5

(c) Draw the layout of the 2 input XNOR gate. 5

5. (a) Describe the rotation operation for a 4*bit* binary word '*B*' $(b_3\, b_2\, b_1\, b_o)$ used for 4*bit* ALU and hence draw the N-MOS switch matrix for 4 *bit* rotate right operation. 2+6

(b) Describe the ROM operation and draw the implementation of ROM array. 2+6

(c) Mention the effect of constant field scaling on these parameters : Intrinsic delay, on-resistance, Acceptor impurity concentration, area. 4

6. (a) Describe the operation of DRAM cell (1 *bit*) with proper circuit diagram and compare the features of SRAM and DRAM. 6+4

(b) Write VHDL code for a full-Adder using 2-Half Adders in a structural model. 10

7. (a) Describe the 4 *bit* multiplication for an 4 *bit* ALU and implement an array based multiplier for this. 10

(b) Describe the operation of Bi-CMOS inverter with circuit diagram. 10
