53 (CS 301) COAR

2016

COMPUTER ORGANIZATION AND ARCHITECTURE

Paper : CS 301

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Question no. ***1*** *is* ***compulsory*** *and answer* ***any four*** *questions from the rest.*

1. Answer the following : 10×2=20

   (a) How to detect an overflow during addition of numbers in 2's complement representation ?

   (b) What do you mean by a program status word ?

   (c) List out the microoperations required for a decode operation of an instruction.

   (d) State the difference between an isolated I/O and memory mapped I/O.

(e) What do you mean by DMA?

(f) Define cycle stealing.

(g) What is virtual memory?

(h) Write the difference between a physical address and a virtual address.

(i) Define hit rate and miss penalty.

(j) What do you mean by locality of reference?

*Answer **any four** questions:*

2. (a) What are the advantages and disadvantages of hardwired and microprogrammed control? Draw the necessary diagram and explain the control signal generation using hardwired control. 4+6=10

(b) Discuss *any five* addressing modes with examples. 5×2=10

3. (a) Given the following memory values and a one-address machine with an accumulator, what value do the following instruction load into the accumulator? 6

- word 20 contains 40

- word 30 contains 50
- word 40 contains 60
- word 50 contains 70

(a) LOAD IMMEDIATE 20

(b) LOAD DIRECT 20

(c) LOAD INDIRECT 20

(d) LOAD IMMEDIATE 30

(e) LOAD DIRECT 30

(f) LOAD INDIRECT 30

(b) What is the difference between post indexing and preindexing? 2

(c) $X = (A + B) * (C + D)$

Write a program to implement the above arithmetic expression using each of the zero address, one address, two address and three address instruction set. 3×4=12

4. *(a)* Explain the characteristics of RISC and CISC architecture. 4+4=8

(b) If the last operation performed on a computer with an 8 bit word was an addition in which the two operands were 00000010 and 00000011, what would be the value of the following flags?

(i) Carry

(ii) Zero

(iii) Overflow

(iv) Sign

(v) Even parity

(vi) Odd parity. 6

(c) Use Booth's algorithm to multiply –7 (multiplicand) by 3 (multiplier), where each number is represented using 4 bits. 6

5. (a) Draw the flowchart for division of unsigned binary numbers. Explain how the algorithm can be modified to divide negative numbers. 5+5=10

(b) What are the different modes of data transfer between the central computer and an external peripheral device? 2

(c) Explain the daisychain priority interrupt with the help of a diagram. 8

6. (a) Explain how data is transferred between memory and a peripheral device in DMA with the help of a diagram. 10

(b) Draw the flowchart and explain the basic communication between a CPU and an I/O processor. 10

7. (a) Explain how the virtual address is converted into real address in a paged virtual memory system. 7

(b) Consider a 32 bit microprocessor that has an on-chip 16-*KByte* four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped? 6+2=8

(c) Suppose a processor has access to two levels of memory. Level 1 (cache) contains 1000 words and has an access time of 0·01s ; level 2 (main memory) contains 100,000 words and has an access time of 0·1s. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose 95% of the memory accesses are found in the cache. Determine the average time to access a word. 5
