53 (EC 602) VLDG

2015

VLSI

Paper : EC 602

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer ***any five*** *questions.*

1. *(a)* What do you mean by Channel length modulation ? Describe and derive the expression for output conductance 'gds' parameter. Draw the Small-Signal model of an *n*-MOS including Channel length-model. 5

   (b) Write a short note on Metallizaiton process. 5

   (c) Implement the following function in CMOS and draw the corresponding layout.

   $$f = \overline{A \cdot B + C \cdot D}$$ 10

2. (a) Discuss the operation of CMOS SRAM cell for reading, writing and holding data. 10

(b) Write a short-note on Bi-CMOS-technology. 5

(c) Write the masking steps required for an *n*-well CMOS technology. 5

3. (a) Derive the expression for threshold voltage of a *n*-MOSFET. 5

(b) Discuss the operation of Bi-COMS inverter using proper circuit diagram. 10

(c) Derive an expression for rise time for an CMOS inverter. 5

4. (a) What do you mean by a data path element? Draw the Architecture for Array multiplier for 4 bit word multiplication. 10

(b) Write down the design-rules for an Active area containing poly layers (λ-based). 5

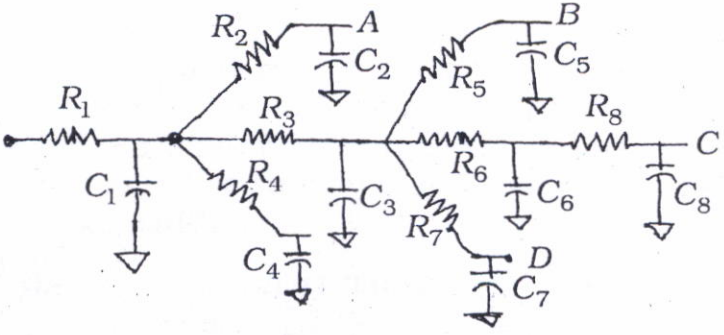
(c) Write a short note on probe testing. 5

5. *(a)* Why scaling is important in IC-design ? Mention the types of scaling and discuss each parameter due to scaling. 10

(b) Draw a typical structure of an FPGA and discuss the Xilinx SRAM based FPGA. 10

6. *(a)* Write down VHDL code for an 4 : 1 MUX using 2 : 1 Muxes using structural model. 10

(b) Calculate Elmore's Delay of the following RC-network shown at nodes 'A' & B, C & 'D'. 10



7. *(a)* Implement the following function in CMOS logic & draw layout for that $f = \overline{A + B \cdot C}$. 10

(b) Write a short note on capacitors in CMOS. 5

(c) Show the internal parasitic capacitances in an *n*-MOS Transistor using cross-sectional view. 5
