53 (EC-401) DGEL

2015

DIGITAL ELECTRONICS

Paper : EC 401

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

Answer ***any five*** *questions.*

1. *(a)* Why are NAND and NOR gates called universal gates ? 2

(b) What are the basic operations in Boolean algebra ? 2

(c) Why is a demultiplexer called a distributor ? 2

(d) How does a J-K flip flop differ from an S-R flip flop in its operation ? 2

(e) What do you mean by an invalid (illegal) state? Give examples. 3

(f) What do you mean by toggling? 2

(g) What are PRESET and CLEAR inputs? 3

(h) Write the procedure to simplify the Boolean expressions using K-maps. 4

2. (a) Implement a full-adder using two 4 : 1 multiplexer. 5

(b) Implement the following expression using a single 8 : 1 multiplexer

$$Y(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$$

5

(c) Draw the simplest possible logic diagram that implements the output of the logic diagrams shown below : 5+5=10

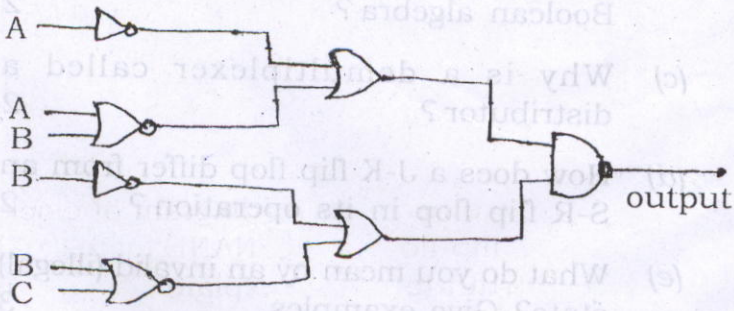

Fig 1(c)

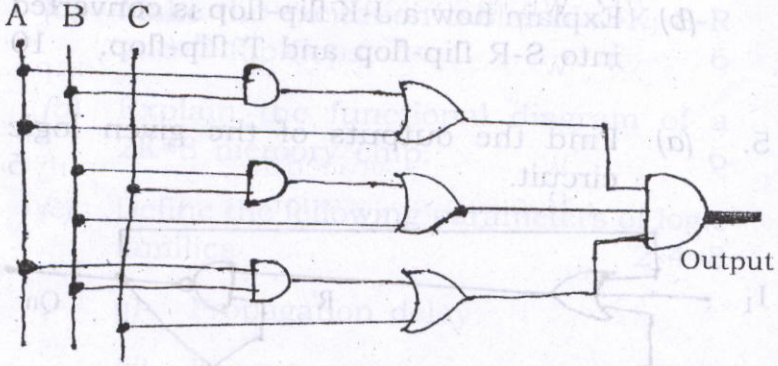

Fig. 2(c)

3. *(a)* What is a comparator ? Design a 2-bit. comparator using logic gates.

2+8=10

(b) Minimize the following Boolean functions and implement it using basic gates only. 10

(i) $Y(A,B,C,D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$

(ii) $f(P, Q, R, S) = \sum m(2, 3, 5, 13, 14) + d(8, 9, 10, 11)$

4. *(a)* Draw a neat circuit diagram of clocked J-K flip-flop using NAND gates. Give its truth table and explain race around condition. 10

(b) Explain how a J-K flip-flop is converted into S-R flip-flop and T flip-flop. 10

5. (a) Find the outputs of the given logic circuit. 6

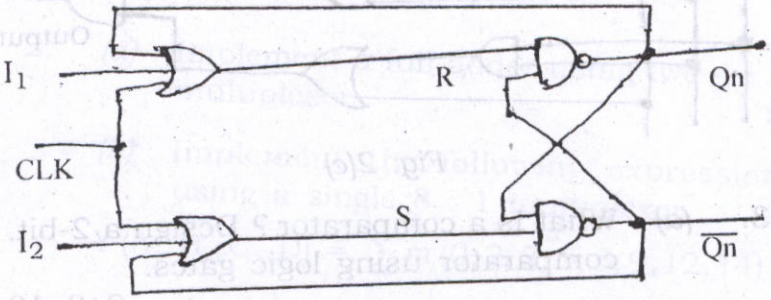

Fig. 5(a) logic circuit

(b) Design and implement a Mod-5 synchronous counter using J-K flip-flop. 8

(c) Design a circuit to generate the sequence $0 \rightarrow 2 \rightarrow 5 \rightarrow 4 \rightarrow 7 \rightarrow 3$. 6

6. (a) Draw the Block diagram of PLA and implement a full adder circuit using PLA having three inputs eight product terms and two outputs. 10

(b) Design a 3 bits Binary to Gray code converter using a suitable PLA. 10

7. *(a)* Make the excitation tables of J-K, S-R and T flip-flops. 6

(b) Explain the functional diagram of a 2K×8 memory chip. 6

(c) Define the following parameters of logic families 2×4=8

(i) Propagation delay

(ii) Fanout

(iii) Noise margin

(iv) Figure of merit.
