53 (IT 303) DLDN

2015

DIGITAL LOGIC DESIGN

Paper : IT 303 (Back)

Full Marks : 100

Time : Three hours

The figures in the margin indicate full marks for the questions.

*Answer **any five** questions.*

1. *(a)* Convert the following

   (i) $(56)_8$ to binary

   (ii) $(15)_{16}$ to binary

   (iii) $(25)_{10}$ to binary

   (iv) $(012)_{10}$ to octal

   (v) $(F_2)_{16}$ to Decimal 5

   (b) Simplify the following using boolean algebra : 2×5=10

   (i) $xy + x'$

(ii) $(x+x')(y+y)(z\cdot\overline{z})$

(iii) $\overline{a+b}\,(\overline{a}\cdot b)$

(iv) $a+abc$

(v) $x(x+y)(x+\overline{y})$

(c) Prove that

(i) $\overline{a\cdot b}=\overline{a}+\overline{b}$

(ii) $\overline{a+b}=\overline{a}\cdot\overline{b}$ 5

2. (a) Draw the logic circuit of below boolean function using basic gates : 2+2+3=7

(i) $Y=(a+b)(c+d)$

(ii) $a'b'+(c+d)xy$

(iii) $Y=a+b'c+d'e(f+g)$

(b) Using only nand gate implement the below boolean function

$Y=ab+bc+cd$ 4

(c) Starting from block diagram and truth table design a 2 to 4 Decoder Circuit. 6

(d) Write down the truth table of a Full Adder. 3

3. (a) Design a Half adder circuit. 5

(b) Write down the function table of a 8 : 1 multiplexer. 3

(c) Write down the truth table of a 4 to 2 encoder. 3

(d) Draw the block diagram of a 3 bit parallel adder. 4

(e) Write down whether the below statements are *true / false*.

(i) It both inputs are logic 1 to a 2 input X-OR gate then the output is going to be logic 1.

(ii) BCD code of Decimal 56 is 101110

(iii) Excess-3 code of 21 is 00110010.

(iv) S-R latch is a combinational circuit.

(v) Multiplexer is a data selector circuit. 5

4. (a) Explain the truth table of a J-K latch. 5

(b) Draw the Block diagram of a Master-Slave flip flop using D-latch as basic block. 3

(c) Draw the circuit of a S-R latch with enable and explain it's operation. 3+5=8

(d) Fill in the blanks : 4

(i) 1 to 4 De-multiplexer, No. of control input needed is _____ .

(ii) D latch, if input is logic 1 output is going to be _____ .

(iii) Half subtractor, inputs are 1, 1 then the output is _____ .

(iv) If both the inputs of a AND gate are logic 1 then output is _____ .

5. (a) Design a Full subtractor circuit. 8

(b) Perform subtraction using 2's complement method 1101-0100. 3

(c) Simplify the below boolean functions using *K*-map method. 4+5=9

(i) $f(w,x,y,z) = \sum m(0, 2, 4, 9, 10, 11, 12, 13)$

(ii) $f(w, x, y, z) = w'x'y'z' + w'x'yz + wx'y'z + wxyz + w'x'y'z + w'xyz'$

4+5=9

6. (a) Explain the operation of a 4 bit register using timing diagram, block diagram etc. 10

(b) Describe the operation of a 2 bit ripple counter with timing diagram, block diagram etc. 10

7. (a) Design a 3 bit counter using D-FF. 12

(b) Write down the excitation table of a J-K FF. 3

(c) What are the main differences between combinational and sequential circuits ? 3

(d) How is excitation table different from that truth table ? 2
