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DEPERTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SIGMA-DELTA ADC FOR BIOMEDICAL APPLICATION

A Project Work Submitted in Partial Fulfilment of the Requirements for Seven Semester B.Tech

In

ELECTRONICS & COMMUNICATION ENGINEERING

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ABSTRACT

This report describes a very brief introduction to the 2nd order Sigma Delta ADC for Biomedical Application up to 150Hz. The sampling theorem and quantization noise theory are reviewed and it is shown that a Sigma Delta ADC grossly oversamples the input signal and shapes the noise spectrum such that the modulator appears to be a high pass filter for the noise and allow pass filter for the input signal. Loop filter is used for noise shaping combining with DAC. We are using two types of 1bit modulator-CIFF and CIFB. The concept of digital part is introduced as incorporated with filtering and downsampler. The digital part is the decimation filter that is implemented by combining one 5th order CIC filter and two FIR filter.

CONTENTS

Chapter 1: INTRODUCTION

Delta-sigma (**ΔΣ**; or **sigma-delta**, **ΣΔ**) modulation is a method for encoding analog signals into digital signals or higher-resolution digital signals into lower-resolution digital signals.

The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. The low-resolution signal typically changes more quickly than the high-resolution signal and it can be filtered to recover the high-resolution signal with little or no loss of fidelity. This technique has found increasing use in modern electronic components such as converters, frequency synthesizers, switched-mode power supplies and motor controllers.

Both analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) can employ delta-sigma modulation. A delta-sigma ADC first encodes an analog signal using delta-sigma modulation and then applies a digital filter to form a higher-resolution digital output. On the other hand, a delta-sigma DAC encodes a high-resolution digital input signal into a lower-resolution signal that is mapped to voltages and then smoothed with an analog filter. In both cases, the temporary use of a lower-resolution signal simplifies circuit design and improves efficiency.

The coarsely-quantized output of a delta-sigma modulator is occasionally used directly in signal processing or as a representation for signal storage. For example, the Super Audio CD (SACD) stores the output of a delta-sigma modulator directly on a disk.

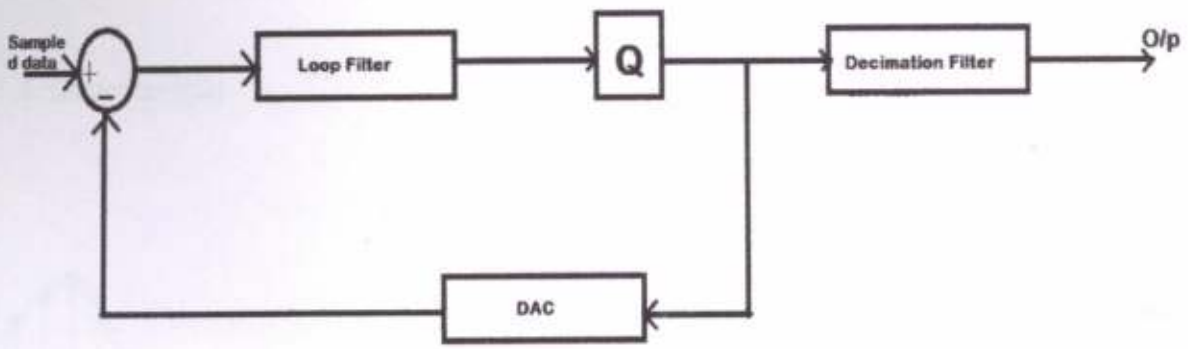


Figure 1: Block Diagram of a Delta Sigma Converter

1.1: Loop Filter

The loop filter is described by an ABCD matrix. For single-quantizer systems, the loop filter is a twoinput, one-output linear system and ABCD is an (n+1)'(n+2) matrix, partitioned into A (n x n), B (n x 2), C (1 x n) and D (1x 2) sub-matrices. This formulation is sufficiently general to encompass all single-quantizer modulators which employ linear loop filters.

1.2: Decimation filter

In audio applications, need for efficient digital filter has been increasing at high rate because of high speed and low power requirements. The oversampling sigma-delta modulation is a proven method to realize high- and very high-resolution analog to digital converters. Need for decimation filter is to remove the quantization noise within the band of interest and avoid aliasing of high

frequency down to low frequency components or within the signal bandwidth. This way of implementation reduces the power consumption, also utilizes much lesser hardware compared to few other designs this is because at each stage the filters operate at a lower sampling rate. comb filter used at the beginning of the decimation filter requires minimal hardware to perform down-sampling to low frequency components from high frequency components. We are discussing design of a decimation filter used for high performance audio applications. We implemented decimation filter in order to obtain low-power with the use of canonical signed digit (CSD) representation. The filter coefficients obtained are represented using CSD representation, which requires less hardware and consumes less power . Basic requirement of this digital filter is to decrease the frequency spectrum and filtered out the feedback signal Because of the use of oversampling in sigma-delta modulators, the need arises for changing the sampling rate of signal, decreasing it to Nyquist rate in A/D-converters. Thus, the high resolution can be achieved by the decimation (sample reduction). Such sample reduction can be achieved employing high precision FIR filters, usually in cascaded structures. This paper describes the steps of practical design of decimation filter for high-resolution ΣΔ A/D converter. The design of a decimation filter is proposed that employs three stage – one Cascaded Integration Comb filter (CIC) followed by two FIR filters. This approach eliminates the need for multiplication, requires a maximum clock frequency equal to the sampling. Finally, it explains how to implement the filter efficiently in hardware.

1.3: DAC

In electronics, a **digital-to-analog converter** (**DAC** or **D-to-A**) is a function that converts digital data (usually binary) into an analog signal (current, voltage, or electric charge). An digital to analog converter (DAC) performs the reverse function of ADC. A DAC is often needed to convert the digital signal to analog, for example to drive an earphone or loudspeaker amplifier and produce sound (analog air pressure waves).

1.4: Quantizer(Q)

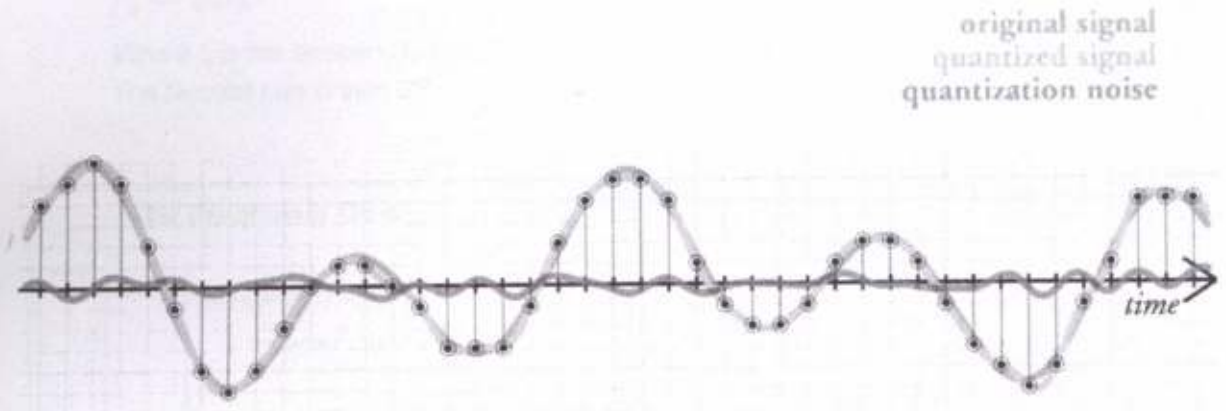


Figure 1.1: Quantizaton

Quantization, in mathematics and digital signal processing, is the process of mapping a large set of input values to a smaller set – such as rounding values to some unit of precision. A device or algorithmic function that performs quantization is called a quantizer. The round-off error introduced by quantization is referred to as quantization error.

In analog-to-digital conversion, the difference between the actual analog value and quantized digital value is called quantization error or quantization distortion. This error is either due to rounding or truncation. The error signal is sometimes considered as an additional random signal called quantization noise because of its stochastic behaviour. Quantization is involved to some degree in nearly all digital signal processing, as the process of representing a signal in digital form ordinarily involves rounding. Quantization also forms the core of essentially all lossy compression algorithms.

Chapter 2: BASICS BLOCKS OF SIGMA DELTA MODULATOR

2.1: Oversampling

The key advantage of oversampling is that the signal band occupies a small fraction of the Nyquist interval making it possible to use digital cancellation on the relatively large fraction of the quantization noise that is outside the band of interest. The use an ideal digital filter after the *A/D* conversion removes the noise from *fB* to *fs*/2 and significantly reduces the quantization noise power by a factor of *fs*/(2*fB*) leading to

where *Vref* is the reference voltage and *n* is the number of bits of the quantizer.

In signal processing, **oversampling** is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled. Oversampling helps avoid aliasing, improves resolution and reduces noise.

An oversampled signal is said to be oversampled by a factor of β, defined as

$$\beta \stackrel{\text{def}}{=} \frac{f_s}{2B}$$

or

$$f_s = 2\beta B$$

Where f_s is the sampling frequency and B is the bandwidth or highest frequency of the signal. The Nyquist rate is then $2B$.

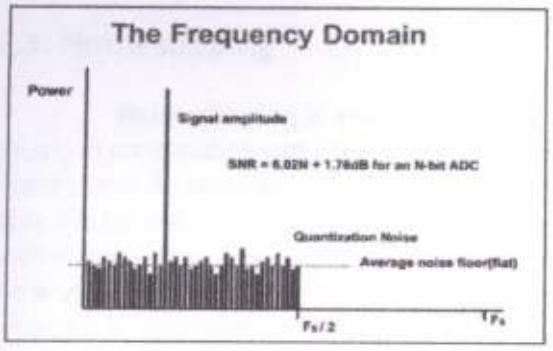


Figure 2: sampling by nyquist interval

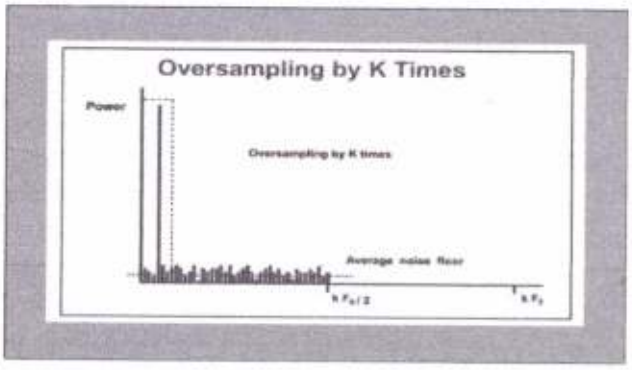


Figure 2.1:over sampling by k times of the nyquist interval

The definition of the equivalent number of bits shows that an oversampling by *OSR* potentially improves the number of bits from *n* to

$$ENOB = n + 0.5 \cdot log2 \cdot (OSR)$$

showing that every increase of the *OSR* by a factor four potentially improves the converter resolution by 1-*bit*. The advantage is not so important as, for example, for gaining 5-*bit* it is necessary to use *OSR* = 1024. Nevertheless, when oversampling is used to relax the anti-aliasing specifications, the additional benefit of obtaining extra bits is obviously positive.

2.2: Quantization and Quantization Error.

Discretization in amplitude domain of any continuous signal is said to be Quantization. This continuous-todiscrete transformation in amplitude generates an error, commonly referred to as quantization error. The quantization itself introduces a fundamental limitation on the performance of an ideal ADC. It degrades the quality of the input signal whose continuous-value levels are mapped onto a finite set of discrete levels.

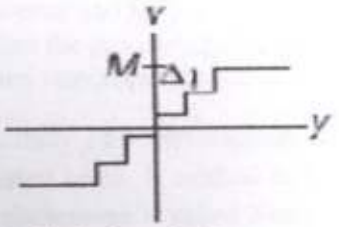


Figure 3: Ideal charactrstics

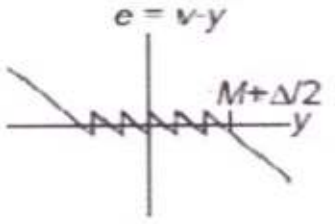


Figure 4: Quantization error

Fig.4 shows the transfer characteristic of an ideal quantizer, where e stands for the quantization error. This error is a nonlinear function of the input signal, as shown in Fig.5. Note that, if x is confined to the full-scale input range [$-X_{FS}/2$, $X_{FS}/2$], the quantization error is bounded by [$-\Delta/2$, $\Delta/2$], with being the quantization step, defined as the separation between adjacent output levels in the quantizer. As long as the quantizer does not overload $|e| \leq \Delta/2$.The number of quantization levels is large, then the quantization noise is white with a power $\sigma e^2 = \Delta^2/12 = 1/3$ for $\Delta=2$.

2.3: Noise shaping

Noise shaping is a technique typically used in digital audio, image, and video processing, usually in combination with dithering, as part of the process of quantization or bit-depth reduction of a digital signal. Its purpose is to increase the apparent signal to noise ratio of the resultant signal. It does this by altering the spectral shape of the error that is introduced by dithering and quantization; such that the noise power is at a lower level in frequency bands at which noise is perceived to be more undesirable and at a correspondingly higher level in bands where it is perceived to be less undesirable. A popular noise shaping algorithm used in image processing is known as 'Floyd Steinberg dithering'; and many noise shaping algorithms used in audio processing are based on an 'Absolute threshold of hearing'.

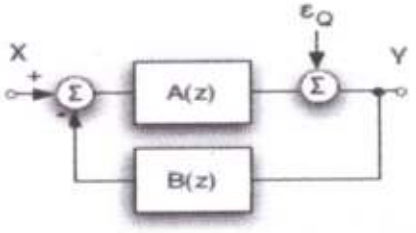


Figure 5: Incorporating the quantizer in a feedback loop

The scheme has a sampled data input that, after the processing block $A(z)$, is converter into digital. For closing the loop it is necessary to generate the analog representation of the converted signal as done by the DAC. A second processing block $A(z)$ is used before the subtracting element. The linear model of Fig:2 represents the quantization error with the additive noise ϵ_Q that is a second input of the circuit.

By inspection of the scheme it results

$$[X - Y \cdot B(z)]A(z) + \epsilon_Q = Y$$

whose solution yields

$$Y = \frac{X(z).A(z)}{1+A(z).B(z)} + \frac{\epsilon_Q}{1+A(z).B(z)}$$

The above equation shows that signal and quantization noise pass through two different transfer functions

$$Y = X \cdot S(z) + \epsilon_Q \cdot N(z)$$

named signal transfer ($S(z)$) function and noise transfer function ($N(z)$) respectively. For a low pass data converter and for securing a beneficial noise shaping, $S(z)$ should be low pass and $N(z)$ high pass. Since often the processing block $B(z)$ is not used ($B(z) = 1$), $A(z)$ must be integrator-type for obtaining the desired responses.tains noise shaping

The accuracy of Oversampling ADC / DAC can be increased by applying methods to reduce quantization noise. A method in which the inband noise is pushed in the frequency out of interest. Such a phenomena is called Noise Shaping ,where the quantization error conceptually generated by the difference of the input signal, , from an analog version of the quantizer output, —is shaped by a filter with a transfer function, usually called noise transfer function (NTF), which can be either of high-pass type or band-stop type. In case low pass oversampled signal ,the low frequency inband component the removal of quantization Noise can be done through Differentiator in z domain transfer function is given by:

NTF (z) = $(1 - z^{-1})^L$. Where L denotes the order of filter.

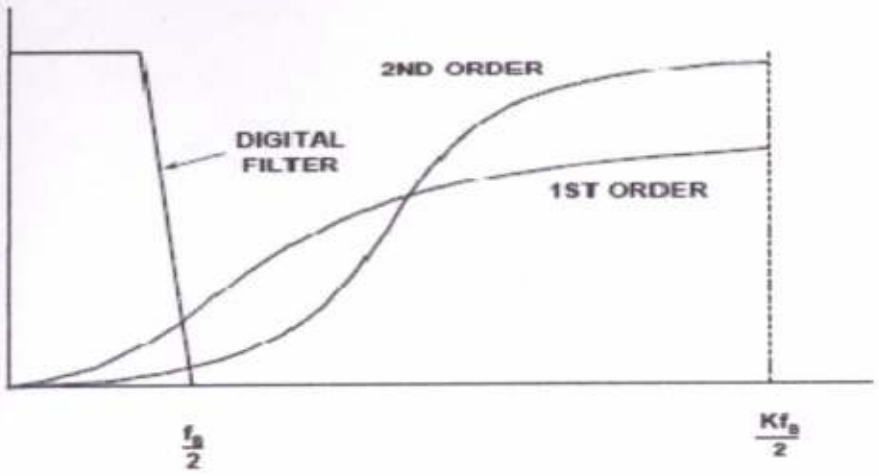


Figure 6:Sigma-Delta modulators shape quantization noise

2.4: Noise shaping and 1-bit converters

Since around 1989, 1 bit delta-sigma modulators have been used in analog to digital converters. This involves sampling the audio at a very high rate (2.8224 million samples per second,

for example) but only using a single bit. Because only 1 bit is used, this converter only has 6.02 dB of dynamic range. The noise floor, however, is spread throughout the entire "legal" frequency range below the Nyquist frequency of 1.4112 MHz. Noise shaping is used to lower the noise present in the audible range (20 Hz to 20 kHz) and increase the noise above the audible range. This results in a broadband dynamic range of only 7.78 dB, but it is not consistent among frequency bands, and in the lowest frequencies (the audible range) the dynamic range is much greater — over 100 dB. Noise Shaping is inherently built into the delta-sigma modulators.

The 1 bit converter is the basis of the DSD formate. One criticism of the 1 bit converter (and thus the DSD system) is that because only 1 bit is used in both the signal and the feedback loop, adequate amounts of dither cannot be used in the feedback loop and distortion can be heard under some conditions. Most A/D converters made since 2000 use multi-bit or multi-level delta sigma modulators that yield more than 1 bit output so that proper dither can be added in the feedback loop. For traditional PCM sampling the signal is then decimated to 44.1 ks/s or other appropriate sample rates.

Chapter 3: Modulator

3.1: General architecture

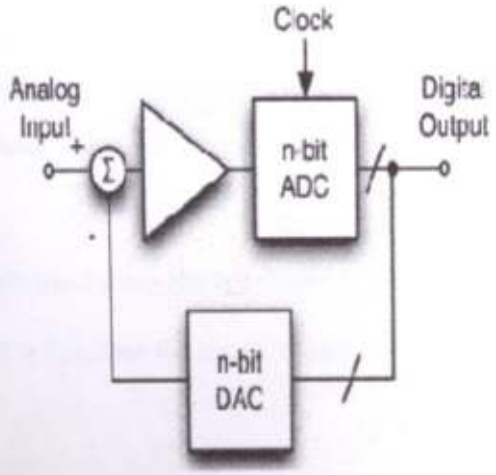


Figure 8: ΣΔ modulator

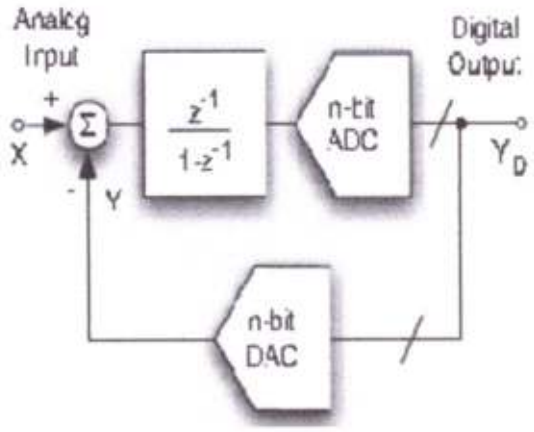


Figure 9: Sampled-data first-order sigma delta modulator

The block diagram of Fig. 8 integrates the difference between the analog input and the *DAC* output to generate the sampled-data input of the *ADC*. The input of the modulator can be already in the sampled-and-hold format or a *S&H* is necessary before the data conversion. In the former case we have a sampled-data ΣΔ, the latter case corresponds to a continuous-time ΣΔ modulator. Moreover, the number of bits used by the *ADC* and the *DAC* distinguishes between a single-bit ΣΔ (or simply ΣΔ) and a multi-bit ΣΔ modulator. Fig. 9 shows the block diagram of sampled-data ΣΔ that uses the transfer function

$$H(z) = \frac{z^{-1}}{1-z^{-1}}$$

to realize the analog sampled-data integration.

Since the quantization associated with the n-bit *ADC* is equivalent to the addition of a quantization error, $\in Q$, and the *DAC* just converts the digital output into a quantized analog signal, then the diagram of Fig. 9 can be modelled with the analog scheme which is a linear sampled-data circuit with two inputs, X and $\in Q$, and one output, Y. The encoder provides a digital representation of the quantized variable Y.

The equation describing the circuit is

$$Y(z) = \{X(z) - Y(z)\}\frac{z^{-1}}{1-z^{-1}} + \in_Q(z)$$

leading to

$$Y(z) = X(z)\, z^{-1} + \in_Q(z)\,(1 - z^{-1})$$

Notice that the signal is just delayed by one clock period while the noise is passed through $(1 - z^{-1})$. This shows that the signal and the quantization noise are processed differently by the modulator. To generalize, we can state that signal passes through the signal transfer function *STF(z)* and the quantization noise through the noise transfer function *NTF(z)*.

$$Y(z) = X \cdot STF(z) + \in_Q(z) \cdot NTF(z).$$

The noise transfer function of the first order ΣΔ is high-pass as is evident by its estimation on the unity circle: $z \rightarrow e^{jwT}$

$$NTF(w) = 1 - e^{-jwT} = 2j e^{-jwT/2} \frac{e^{jwT/2} - e^{-jwT/2}}{2j}$$

$$NTF(\omega) = 2j \; e^{-jwT/2} \; \sin(wT/2)$$

The result shows that the white spectrum of the quantization noise is amplified by 4 but is shaped by $\sin(wT/2)$ giving rise to a significant attenuation of the low-frequency components of the spectrum.

If a digital filter removes any noise power outside the signal band, then the resulting square noise voltage is the integral of the shaped spectrum extended from 0 to f_B.

$$V_n^2 = v_{n,Q}^2 \int_0^{fB} 4 * sin^2(\pi f T)\, df \cong v_{n,Q}^2 \frac{4\pi^2}{3} f_B^3 T^2$$

obtained using the approximation $sin(x) \cong x$, valid for $w_B T/2 \ll \pi/2$. Since $v_{n,Q}^2 = v_{n,Q}^2 f_s/2$ and $T = 1/fs$, then the above equation can be rewritten as

$$V_n^2 = v_{n,Q}^2 \frac{\pi^2}{3} \left[\frac{f_B}{\frac{f_s}{2}}\right]^3 = v_{n,Q}^2 \frac{\pi^2}{3} OSR^{-3}$$

If the *ADC* uses k thresholds, the *DAC* generates k+1 levels in the reference range $0 - Vref$

$$V_{DAC}(i) = i \; v_{ref}/k; \quad i = 0 \ldots\ldots\ldots k.$$

The cascade of *ADC* and *DAC* gives rise to a quantizer whose quantization interval is $\Delta = Vref/k$, and has $nQ = log2(k + 1)$ bits. Moreover, since the power of the quantization noise and that of a full-scale sinewave are respectively

$$v_{n,Q}^2 = V_{ref}^2/k^2 12; \; V_{sine}^2 = V_{ref}^2/8$$

then the maximum *SNR* of the first order ΣΔ modulator is given by

$$SNR_{\Sigma\Delta,1} = \frac{12}{8} . k^2 \frac{3}{\pi^2} OSR^3$$

Assuming $n' = log2k$, above equation in *dB*, becomes

$$SNR_{\Sigma\Delta,1}\,|_{dB} = 6.02\, n' + 1.78 - 5.17 + 9.03 \; \log_2(OSR)$$

3.2: Lee criterion for stability of single-bit modulators

A binary sigma-delta modulator is likely to be stable if $\max |H(e^{jw})| < 2$. Neither necessary nor a sufficient condition but still useful.

$\max |H(e^{jw})|$ is the maximum gain of NTF over all frequencies (remember that w is periodic with period of 2π or H is periodic over f:[0,fs]).

$\max |H(e^{jw})| < 1.5$ is also called H-infinity or $\|H\|_\infty$.

3.3: General architectures for single-quantizer modulators

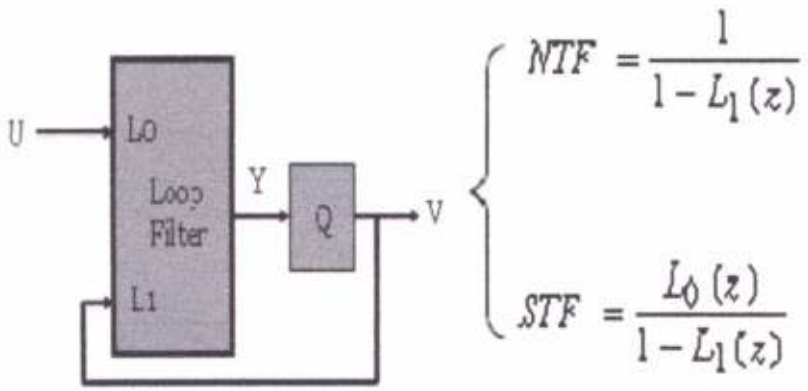


Figure10: Loop filter with one bit quantizer

3.3.1: Loop filters with distributed feedforward and input coupling (CIFF)

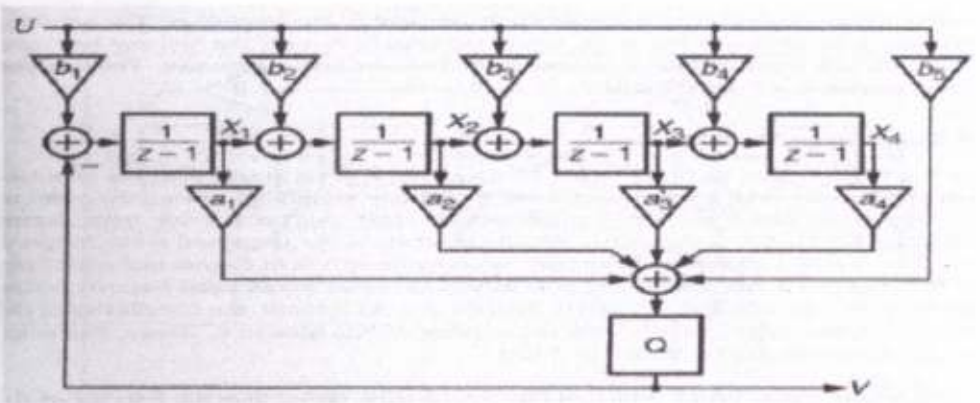


Figure 11: Chain of integrators with weighted feedforward summation

$$L_1(z) = -a_1 I(z) - a_2 I(z)^2 - \cdots - a_N I(z)^N \qquad I(z)=\frac{1}{(z-1)}$$

$$L_0(z) = b_1(a_1 I + a_2 I^2 + \cdots a_N I^N) + b_2(a_2 I + \cdots + a_N I^{N-1}) + \cdots + b_{N+1}$$

For low-distortion architecture, STF=1 $\quad b_2 = b_3 = \cdots = b_N = 0 \quad b_1 = b_{N+1} = 1$

3.3.1.1: Simulink model

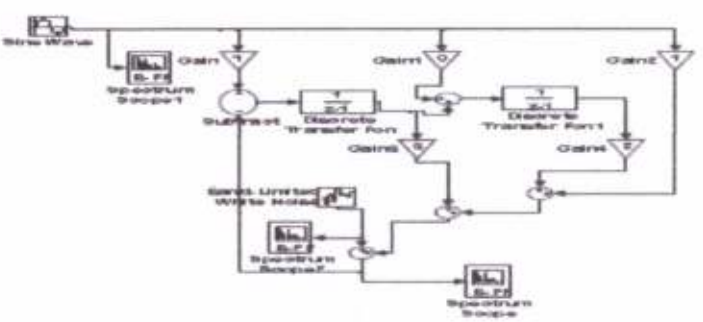


Figure 12: CIFF

3.3.1.2: Simulated result

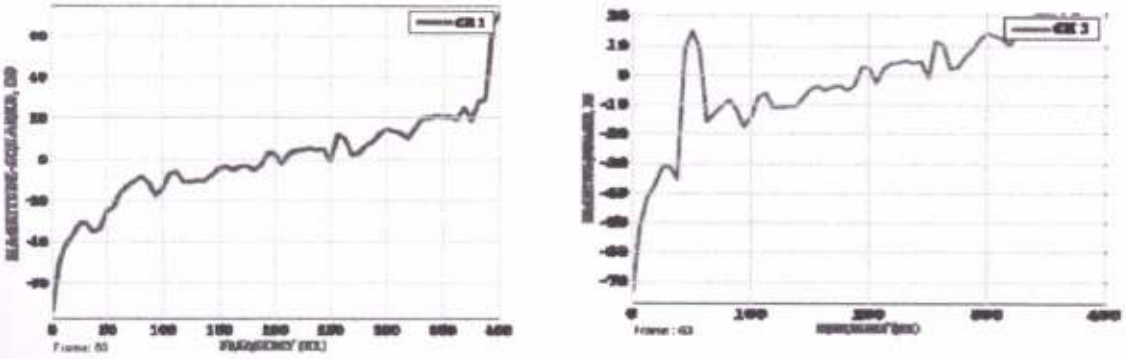


Figure 13: NTF & simulated output

3.3.2: Loop filters with distributed feedback and input coupling (CIFB)

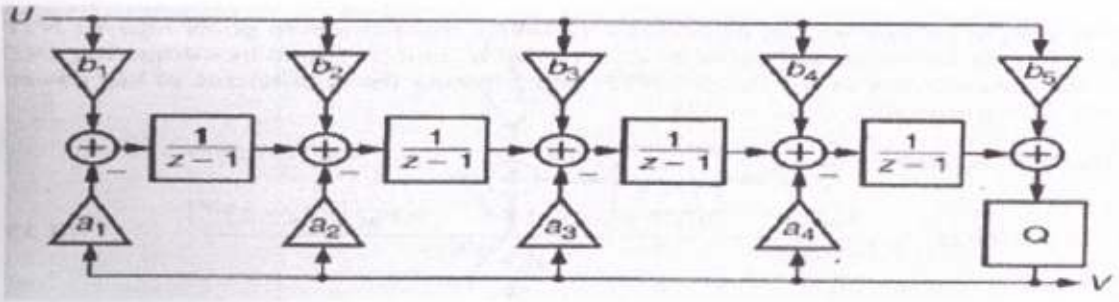


Figure 14: Cascade of 4 integrators with distributed feedback and distributed coupling

$$stf = \frac{L_0(z)}{1 - L_1(z)} = \frac{b_1 + b_2(z-1) + \cdots + b_{N+1}(z-1)^N}{D(z)}$$

All NTF zeros are at DC (z=1)

Poles of NTF and STF are controlled by a_i coefficients (used to control stability). Zeros of STF are controlled by b_i coefficients.

$$L_0(z) = \frac{b_1 + b_2(z-1) + \cdots + b_{N+1}(z-1)^N}{(z-1)^N}$$

Feedforward transfer function

$$L_1(z) = -\frac{a_1 + a_2(z-1) + \cdots + a_N(z-1)^{N-1}}{(z-1)^N}$$

Feedback transfer function

$$ntf = H(z) = \frac{1}{1 - L_1(z)} = \frac{(z-1)^N}{D(z)}$$

$$D(z) = a_1 + a_2(z-1) + \ldots + a_N(z-1)^{N-1} + (z-1)^N$$

Then STF=1 and input to any of the integrators in the loop does not contain input signal component which results in a low distortion architecture.

3.3.2.1: Simulink model

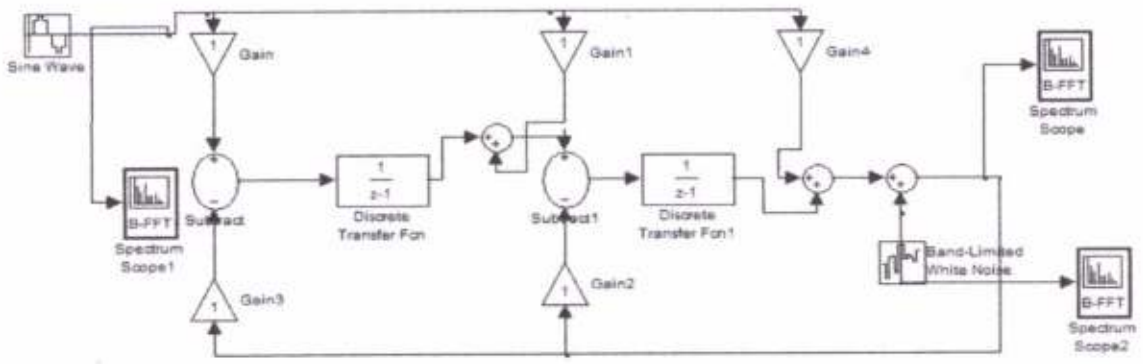


Figure 15: CIFB

3.3.2.2: Simulated result

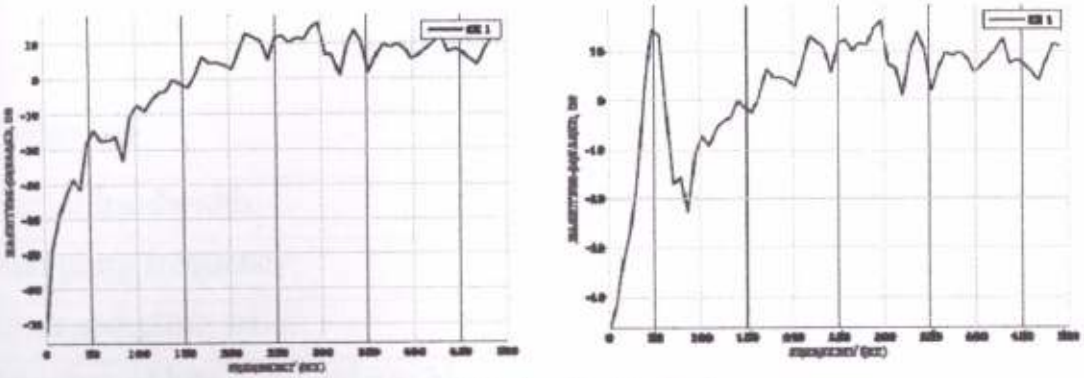


Figure 16: NTF & simulated output

3.4: COMPARISON TABLE FOR DIFFERENT SIGMA DELTA MODULATOR TOPOLOGY

Sr. No.	OSR	Effective number of bits(in bits)	
		CIFF	CIFB
1	2	3.09	2.17
2	4	3.98	3.15
3	8	5.07	5.6

Table 1: Comparision between OSR & ENOB

Chapter 4: Decimation filter

4.1:SPECIFICATION OF THE DECIMATION FILTER FOR SIGMA DELTA CONVERTER

A sigma-delta A/D-converter consists of a sigma-delta modulator, which produces the bitstream at the sampling rate, which can be in the megahertz range. The figure shows a digital side of sigma-delta modulator. The specifications of the decimation filter are dependent upon the overall specification from the sigma-delta converter.

The output of sigma-delta modulator is a 1-bit data bitsteam at the sampling rate, which is 800Hz. The purpose of digital-and-decimation filter (Fig) is to extract information from this data bitstream and reduce the data rate to a more useful value.

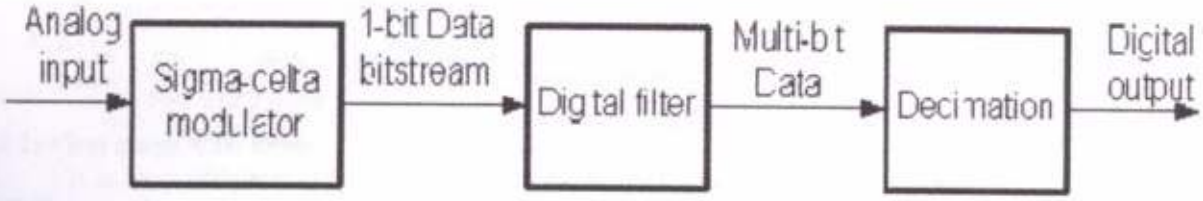


Fig: Sigma-Delta ADC

Parameter	Symbol	Value
Signal bandwidth:	BW	100Hz
Sampling frequency:	Fs	800Hz
Over sampling ratio:	OSR	8
Number of bits in modulator bit stream:	Bmod	1
No of bits in output of filter:	B	7
Passband frequency:	Fpass	100Hz
Stopband frequency:	Fstop	125Hz

Table: Decimation filter specification

Using specification given in above Table , in sigma-delta ADC, the digital filter average the 1-bit data stream, improves the ADC resolution and removes quantization noise that is outside the band of interest. The purpose of decimation filter is to remove the noise shifted by modulator to high frequencies, reduce the sampling frequency of 800Hz and increase the number of bits in the output. With 7 bits in the output of the filter Signal to Noise Ratio (SNR) is 86 dB.

4.2:DESIGN OF THE DECIMATION FILTER

Practically it is complicated to implement a decimation filter in hardware level. It is therefore necessary to use multistage approach, whereby the decimation is performed in several stages. The decimation is done by using two types of decimation filter-Cascade integration Comb(CIC) filter and Finite Impulse Response(FIR) filter. Here we are using 5^{th} order decimation filter with three stages:

- Cascade Integration Comb(CIC) filter where sampling frequency is decimated by a factor 4.
- 1^{st} FIR filter with decimation factor 2. It compensate the in band attenuation introduced by the comb stage.

• 2^{nd} FIR filter with decimation factor 1. It is used for last stage with step transition, to provide the required stop band attenuation.

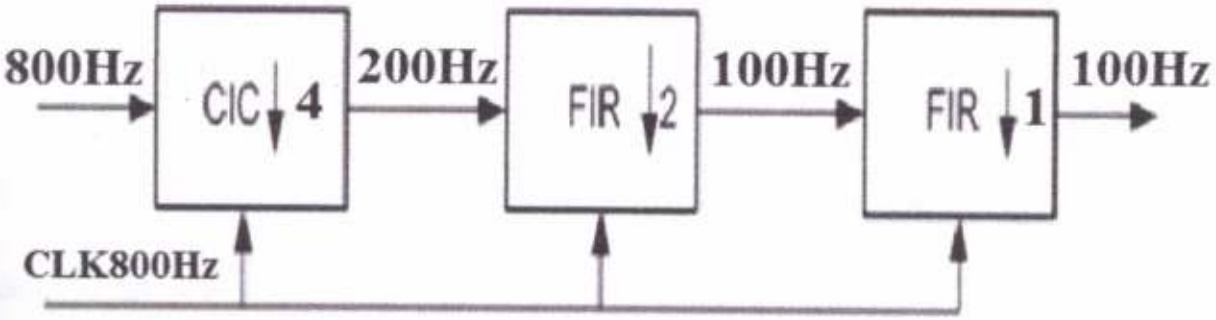


Fig : Decimation filter architecture

4.2.1: First stage, CIC filter

It is very efficient to use a Cascaded Integrated Comb filter (CIC) for the first stage. Such CIC filter can be easily implemented in hardware, requiring no multiplication. Furthermore, it can be used to decimate the data by a large factor, allowing easier implementation of the following stages. The drawback is the drop in the pass-band due to the sin(x)/x response of the filter. This needs to be compensated for in the following stage of FIR filtering. In this design is used CIC filter to decimate data by decimation ratio 4. This filter is mainly consisting of two sections- integration section and comb section.

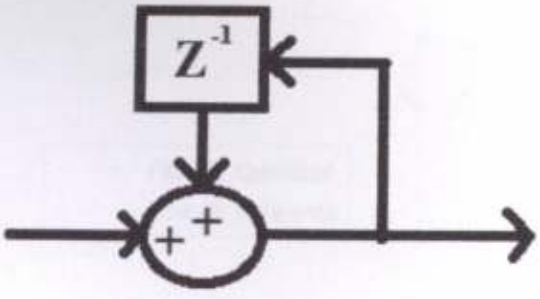


Fig: Integrator

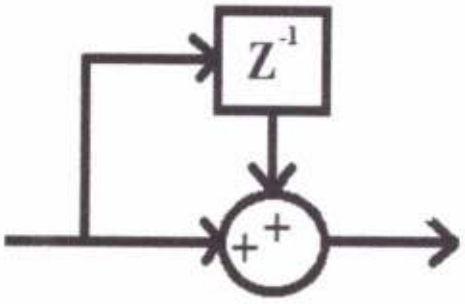


Fig: Comb

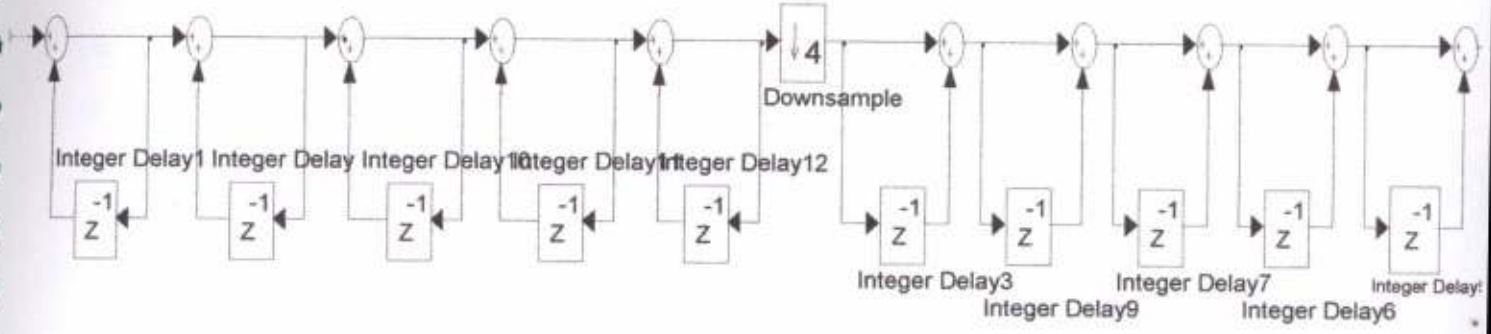


Fig: 5th order CIC block diagram

If N is the order of filter, R is the decimation factor and M is the differential delay then,

N=5 ; R=4 ; M=1

The transfer function for integration section is

$$H_I(z)=\frac{1}{1-z^{-1}}$$

The transfer function for comb section is

$$H_c(z) = 1 - Z^{-RM}$$

The transfer function of the CIC filter is

$$H(z)= H_I(z)H_c(z) = \frac{(1-Z^{-RM})^N}{(1-Z^{-1})^N} = [\sum_{i=0}^{RM-1} Z^{-i}]^N$$

And magnitude of the frequency response,

$$|H(e^{jw})| = |\frac{\sin(\pi Mf)}{\sin\frac{\pi f}{R}}|^N$$

In our proposed CIC filter, N=5, R=16 & M=1

Therefore, $H(z)=[\frac{1-Z^{-16}}{1-Z^{-1}}]^5$

And magnitude of the frequency response,

$$|H(e^{jw})| = |\frac{\sin(\pi Mf)}{\sin\frac{\pi f}{R}}|^N$$

$$= |\frac{\sin(3.14*1*f)}{\sin\frac{3.14*f}{16}}|^5$$

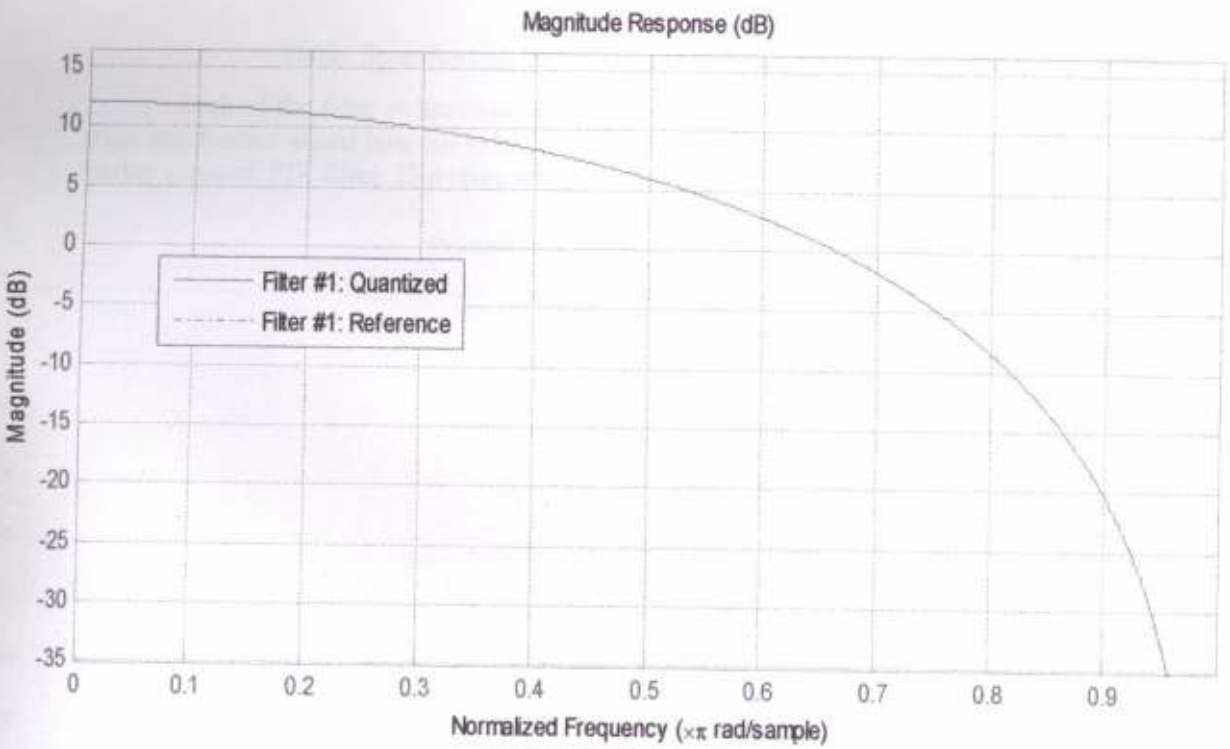


Fig: CIC filter output

4.2.2:Two stages of FIR filtering

The numbers of FIR stages required by looking at computational effort required for different solution and selecting the best one. The frequency band attenuation for each stage can be determined using the following formula:

Passband: $0 \le f \le F_p$

Stopband: $F_i - F_s/2M < f < F_{i-1}/2$

Ripple $_{passband}$: $\delta_p/1$

Ripple $_{Stopband}$: δ_s

where:

Fs: Sampling frequency of filter
I: Total number of stage
Fi= F_{i-1}/Mi*; i is number of stage, (i=1, 2, ... I);*

Filter parameter	**1st FIR**	**2nd FIR**
Sampling frequency(Fs):	200Hz	100Hz
Passband frequency(Apass):	100Hz	100Hz
Stopband frequency(Astop):	375Hz	125Hz
Passband maximum ripple:	0.00025dB	0.00025
Stopband attenuation:	90dB	90dB

Table: Specification for two stages FIR filter

Each of the filter in hardware using only one multiplier. Therefore increasing the number of stage any further would turn out to be less efficient since it would require an extra multiplier for each further stage of FIR filter. Therefore are chosen to use two stage of FIR filter.

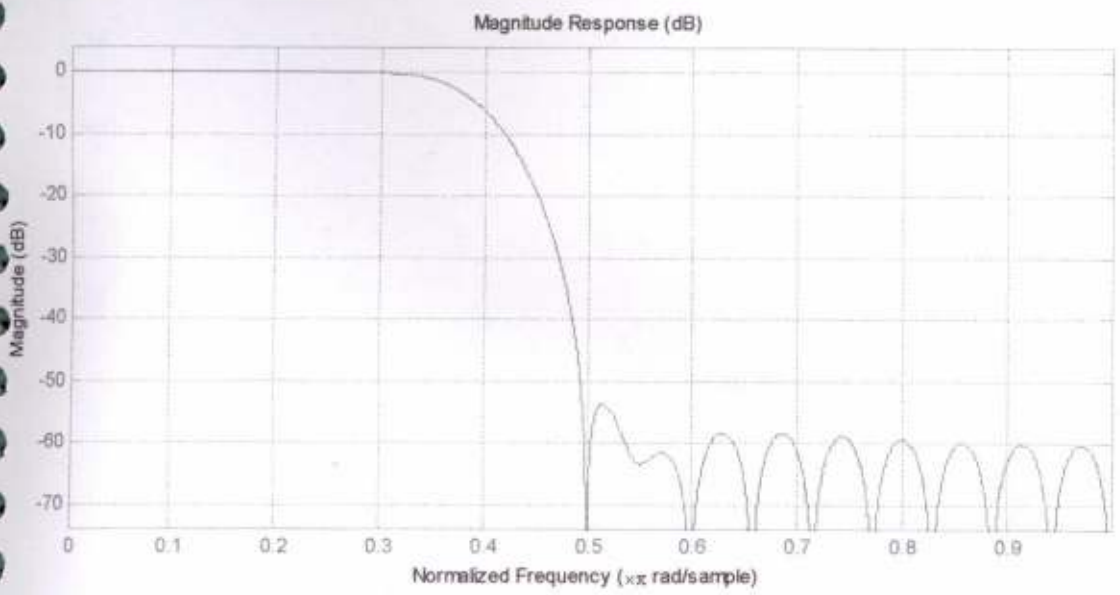


Fig 6: FIR filter respons

4.3:Response of decimation filter

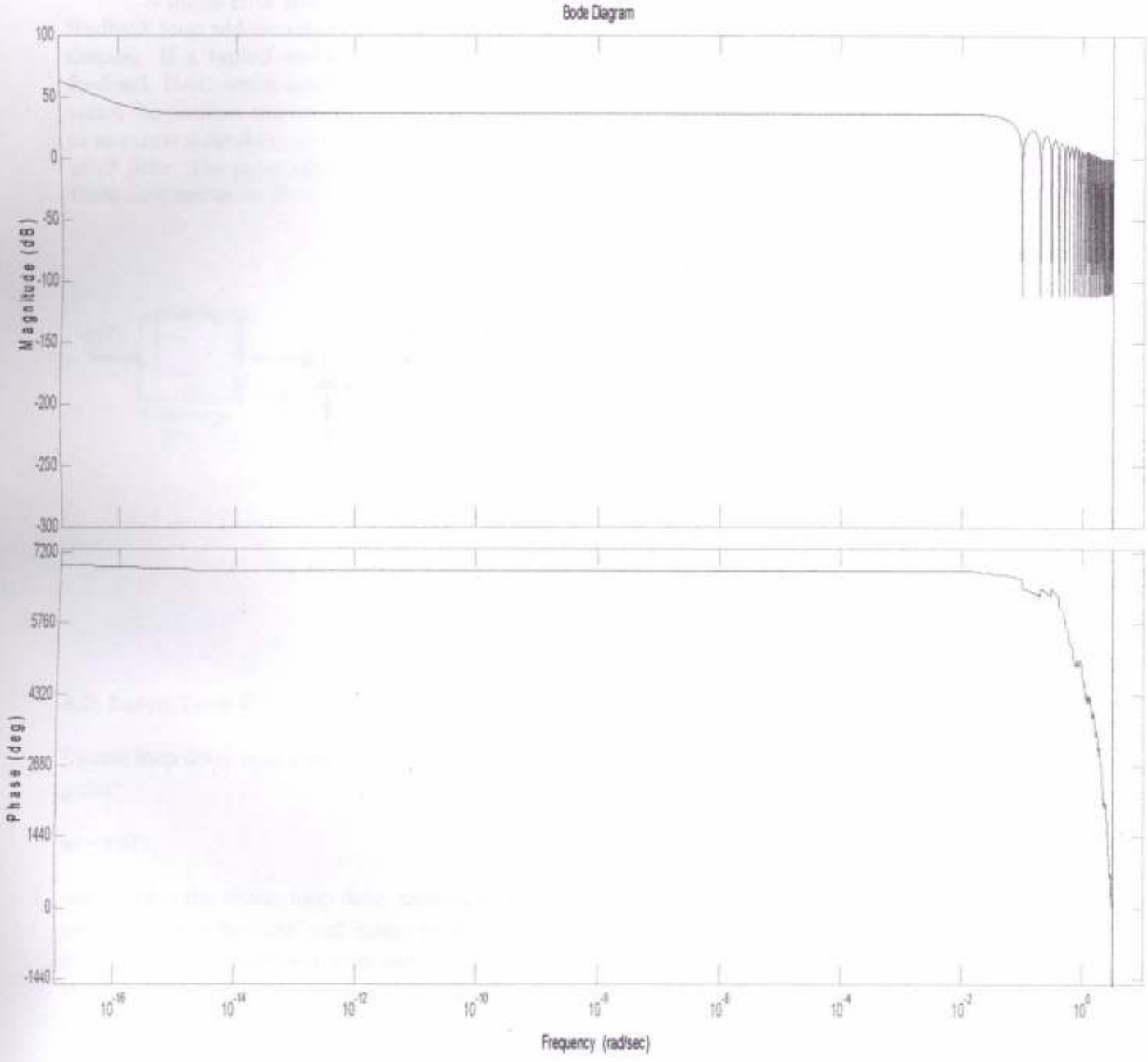


Fig: Decimation filter response

Chapter 5: DAC

5.1: Feedback DAC nonidealities

A major error contributor to CT $\Delta\sum$ modulators is the feedback DAC. Errors in the outermost feedback loop add directly to the input signal, which means that these errors are not subject to noise shaping. If a typical rectangular feedback form is assumed (e.g. NRZ and RZ), most common feedback DAC errors can be derived. The feedback pulse can be affected by timing errors which varies the position and length of the pulse. This can be a constant delay τ_d of the pulse often referred to as *excess loop delay*, or a statistical variation of the position or length of the DAC pulse caused by *clock jitter*. The pulse edges would also inevitably have nonideally rising and falling times due to finite slew rate in the DAC.

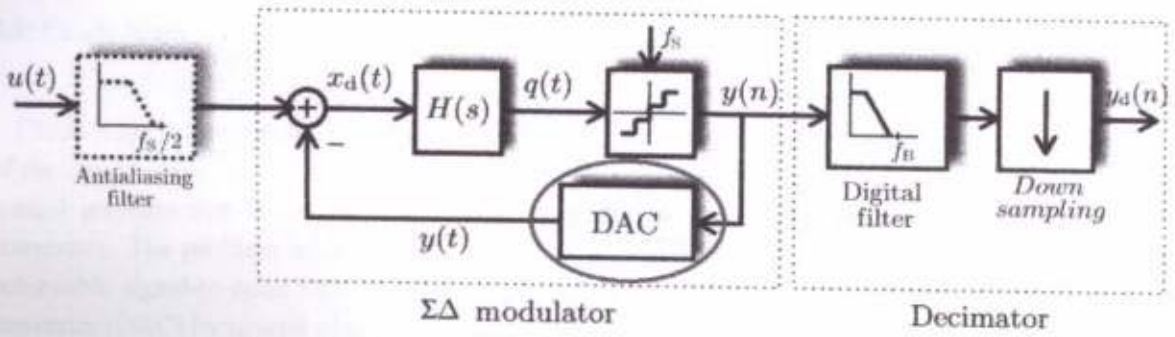


Fig 1: Block diagram of general CT ADC showing feedback DAC.

5.2: Excess Loop Delay

Excess loop delay is an unwanted delay td between the ideal and the implemented feedback DAC pulse:

td = τdTs;

where τd is the excess loop delay relative to the sampling period Ts. This delay can arise from finite respond time in the DAC and delays in the path between the quantizer and the DAC. The excess loop delay causes two different nonideal effects in CT $\Delta\sum$. modulators. When the loop delay shifts the DAC pulse, but the pulse retains within its sampling period or when the loop delay shifts parts of the DAC pulse into the next sampling period. The latter happens when using a NRZ-DAC or even sometimes with RZ-DACs in high speed modulators.

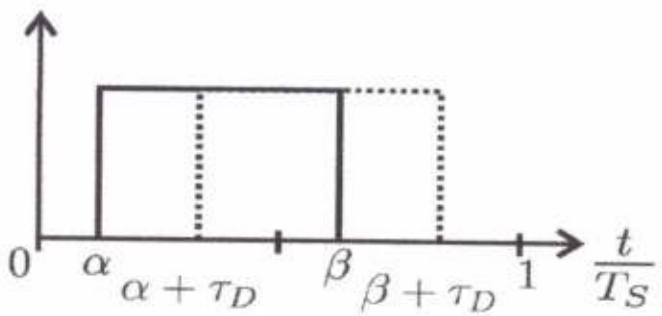


Figure 2: Excess loop delay in RZ DAC

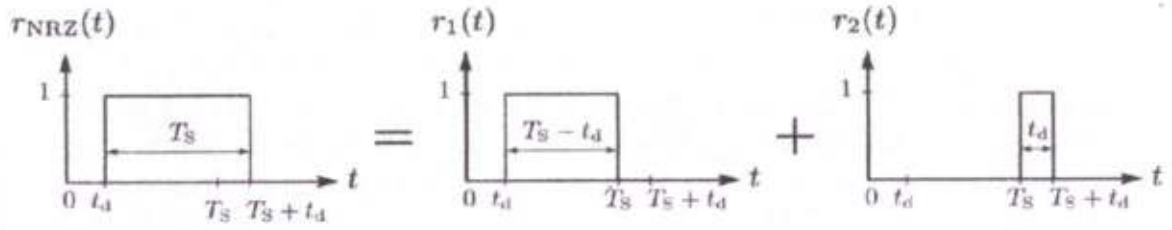


Figure 3: Excess loop delay in NRZ DAC

5.3: Clock Jitter

Clock-jitter is a common problem associated with clock generators due to uncertainty in the timing of the clock edges caused by the finite phase-noise (PN) in the generated clock waveform. It is a critical problem that is becoming the main limitation in the performance of state-of-the-art data-converters. The problem of clock-jitter is a very critical issue and can significantly deteriorate the achievable signal-to-noise ratio (SNR) of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) by several dBs.

Clock jitter introduces errors into both the forward path (as *sampling errors* at the quantizer input) and the feedback path (as *time-delay errors* in the DAC feedback pulses).

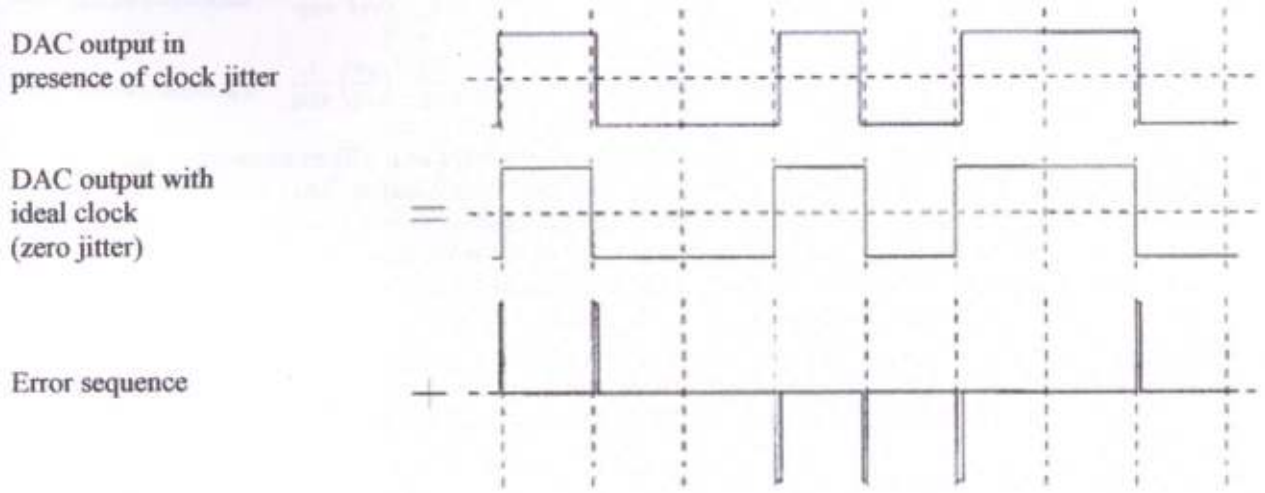


Figure 5.4. Equivalent representations of a jittered bit stream.

5.4:Return-To-Zero DAC Waveforms

Return-to-zero DAC waveforms are known to be robust to even-order nonlinearities resulting from mismatch between rise and fall times, as well as less sensitive to excess loop delay in the quantizer compared to NRZ waveforms. They are the most sensitive to PWJ because the additive jitter induced errors are linearly proportional to the random timing errors at the rise and fall edges every clock-cycle, as illustrated in Figure 15(a). The equivalent error induced by PWJ in a RZ DAC waveform is given

$$\epsilon_j(n) = \frac{\Delta A(n)}{Ts} = (n)\frac{Ts}{Tc}\frac{(\Delta tr(n)+\Delta tf(n))}{Ts}, \quad (1)$$

where $\Delta(n)$ is the area difference resulting from the error in the total integrated charge per one clock period Ts between the ideal and the jittered waveforms, $y(n)$ is the modulator output at the *nth* clock cycle, TC is the duty-cycle of the RZ pulse, and $\Delta tr(n)$ and $\Delta tf(n)$ are the random timing errors in the rise and fall edges, respectively, of the *nth* DAC pulse. For a single tone ig. $\sin(\omega sigt)$ at the input of the $\Delta\square$ modulator, the integrated in-band jitter-induced noise power (*IBJN*) for a RZ DAC is given by

$$IBJN|_{RZ} = \frac{2}{OSR}\left(\frac{e_j}{Tc}\right)^2\left[\frac{{V_{sig}}^2}{2} + \frac{\Delta^2}{12}\frac{1}{2\pi}\int_{-\pi}^{\pi}\left|NTF\left(e^{jw}\right)\right|^2 dw\right] \quad (2)$$

where σj is the rms jitter in the DAC sampling-clock, OSR is the oversampling ratio of the modulator, Δ is the quantization step of the loop quantizer, and NTF is the noise transfer-function of the modulator. From equation (2), the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

$$IBJN|_{RZ,\ due\ to\ input\ signal} = \frac{{V_{sig}}^2}{OSR}\left(\frac{e_j}{Tc}\right)^2 \quad (3)$$

$$IBJN|_{RZ,\ due\ to\ shaped\ noise} = \frac{1}{OSR}\left(\frac{e_j}{Tc}\right)^2\frac{\Delta^2}{12\pi}\int_{-\pi}^{\pi}\left|NTF(e^{jw})\right|^2 dw \quad (4)$$

From the expression in (2), it is evident that the IBJN decreases proportionally with the OSR and the duty cycle of the DAC pulse. Particularly, 1) as the OSR increases, the power spectral density (PSD) of the PWJ induced errors is reduced and hence the resulting integrated in-band noise is decreased accordingly, 2) the additive error in the amount of integrated charge in the loop filter varies linearly with the PWJ at the rise and fall edges by a factor roughly equal to the pulse amplitude, which is inversely proportional to Tc. The IBJN due to in-band signal component, given in (3), causes sidebands of the input signal to appear in the desired band. Also, from (4), PWJ randomly modulating shaped noise results in noise folding back over the desired band and hence elevating the in-band noise level. In (2) and (4), the effect of the quantizer resolution is implicitly included in Δ^2.

5.5:Non-Return-To-Zero DAC Waveforms

Non-return-to-zero DACs are known to be highly sensitive to excess loop delay and also they result in even-order nonlinearities due to mismatch between rise and fall times, in contrast to RZ DAC waveforms. However, they are commonly used in CT $\Delta\square$ modulators due to their simple implementation, relaxed SR requirement on the integrating amplifiers, and lower sensitivity to clock-jitter compared to RZ DACs. In NRZ waveforms the clock-jitter will be effective only during the clock edges at which data is changing. Equivalent error induced by clock-jitter in a NRZ waveform is given by

$$\epsilon_j(n)=\frac{\Delta A(n)}{Ts}=((n)-y(n-1))\frac{\Delta t(n)}{Ts} \quad (5)$$

where $\Delta t(n)$ is the random timing error in the clock edge of the *nth* clock-cycle. For a single tone $Vsig$.$sig(\omega sig\ t)$ at the input of the $\Delta\square$ modulator, the total IBJN for a NRZ DAC is given by

$$IBJN\,|_{NRZ}=4.OSR.\ \mathrm{BW}^2.\sigma_j^2\left[\frac{\pi^2}{2}\left(\frac{{V_{sig}}^2}{{OSR_{sig}}^2}\right)+\frac{\Delta^2{\sigma_{NTF,RMS}}^2}{12}\right]$$

$$\leq 2\pi^2\frac{{V_{sig}}^2.BW^2.\sigma_j^2}{OSR}+\frac{OSR.BW^2.\Delta^2.{\sigma_{NTF,RMS}}^2.\sigma_j^2}{3} \quad (6)$$

where BW is the input signal bandwidth, OSRsig the ratio of the sampling frequency to double the input signal frequency, and

$${\sigma_{NTF,RMS}}^2=\frac{1}{\pi}\int_{-\pi}^{\pi}\left[\left|NTF\left(e^{jw}\right)\right|^2.(1-\cos w)\right]dw$$

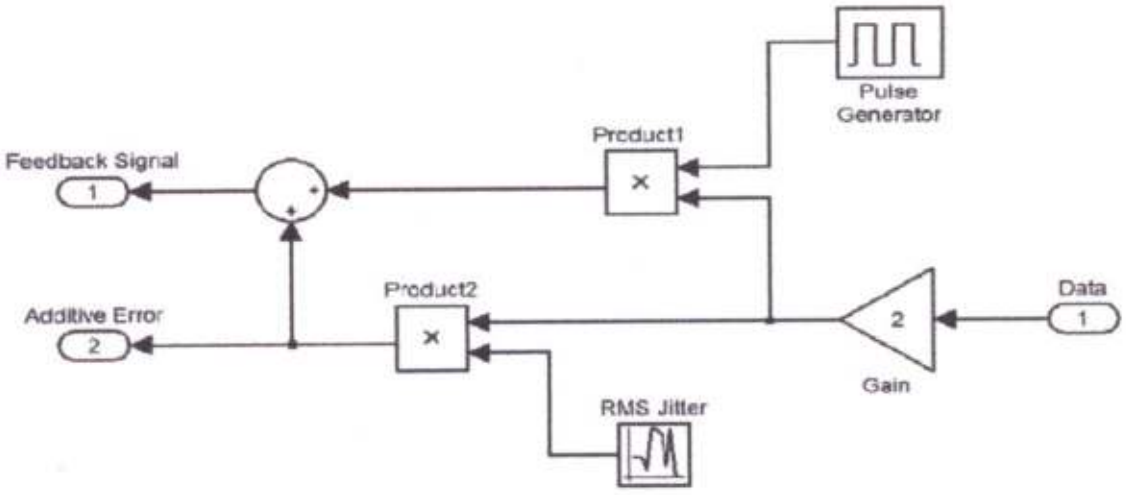
Thus, the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

$$IBJN|_{NRZ,\ due\ to\ signal}\leq 2\pi^2\frac{{V_{sig}}^2.BW^2.\sigma_j^2}{OSR} \quad (7)$$

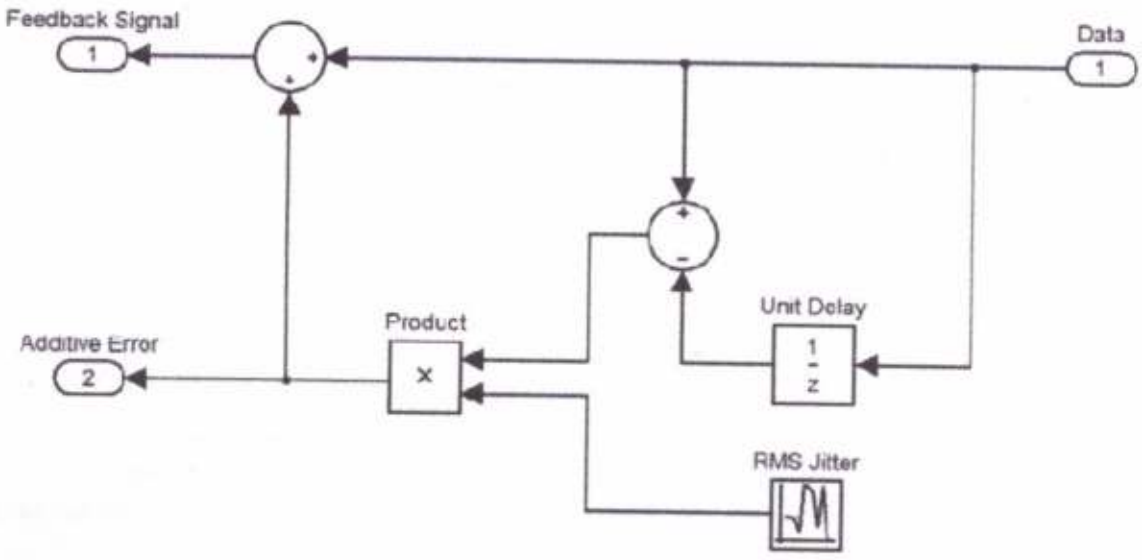
$$IBJN|_{NRZ,\ due\ to\ shaped\ noise}=\frac{OSR.BW^2.\Delta^2.{\sigma_{NTF,RMS}}^2.\sigma_j^2}{3} \quad (8)$$

From the expression in (7), the IBJN due to signal is inversely proportional with the OSR because, intuitively, as the OSR increases, less signal-related transitions will occur at the modulator output and hence less additive jitter noise will be generated. On the other hand, from (8), the IBJN due to shaped noise increases proportionally with the OSR because a higher OSR means more OOB shaped noise components will be modulated and fold back over the desired channel by the PN components at their respective frequencies. Therefore, the OSR needs to be optimized for better robustness to PWJ according to the contribution of each component (in-band signal and shaped noise). Also, the IBJN due to shaped noise is proportional to ${\sigma_{NTF,RMS}}^2$, and thus to minimize the PWJ, the aggressiveness of the NTF needs to be relaxed.

5.6: Modelling for DAC Jitter



(a)



(b)

Fig 4: FIG 5: Simulink Modeling for DACs and jitter induced additive errors in the feedback of a CT Δ□ modulator. (a) RZ DAC. (b) NRZ DAC.

Conclusion & future work

Conclusion

From the aforementioned results, it is concluded that sigma delta adc provide us perfect digital form bio-medical signal. The OSR increases the SNDR and ENoB also increases, after a certain level the increase in OSR will not affect the SNR value. For both the topology of cascade of integrators and cascade of resonators , the values for feedforward and feedback form are approximately same .Also for higher OSR (above OSR = 8) ,the values obtained for SNDR and ENoB is higher in the case of cascade of resonators than cascade of integrators for both feedforward and feedback form.

Future work

We have implemented sigma-delta adc for bio-medical application which has the bandwidth of 150Hz. We are trying to upgrade our design so that it will be suitable for audio applications having bandwidth of 20kHz by applying more order of the modulator.

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